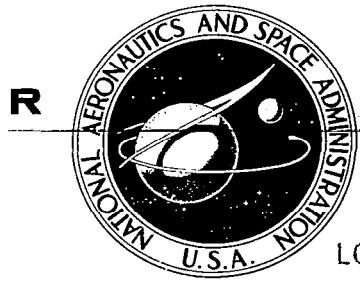
NASA CONTRACTOR REPORT



NASA CR-74

A REENTRY VOICE COMMUNICATION SYSTEM FOR USE IN CONJUNCTION WITH RADAR TRACKING EQUIPMENT

Prepared under Contract No. NASw-586 *by*
AVCO CORPORATION
Wilmington, Massachusetts
for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION • WASHINGTON, D. C. • JULY 1964

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TABLE OF CONTENTS

TABLE OF CONTENTS (cont.)

TABLE OF CONTENTS (cont.)

TABLE OF CONTENTS (Cont.)

TABLE OF CONTENTS (Cont.)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Cont.)

LIST OF ILLUSTRATIONS (Cont.)

LIST OF ILLUSTRATIONS (Cont.)

LIST OF TABLES

SECTION I

SUMMARY

This document is the final report on work performed by the Research and Advanced Development Division of Avco Corporation (Avco-RAD) for the National Aeronautics and Space Administration (NASA) under the terms of Contract Number NASw-586.

The design and development of the Astrovoice II space communications system is described in considerable detail. This system is capable of transmitting encoded voice or other data from a vehicle in space to one or more ground stations via a radar link which is simultaneously used for vehicle tracking. A pulse position modulation technique is used in encoding data for transmission.

Use of this system in conjunction with radar tracking equipment operating at C-band frequencies enables communication to be maintained during hypersonic re-entry despite the plasma-induced signal attenuation accompanying such re-entry. In addition, advantageous, non-interfering secondary use is made of available radar tracking equipment.

The Astrovoice II system has excellent potential for deep space probe communication applications, particularly for transmission of low information rate (less than 3 kilocycles per second), pulse position modulated data.

The investigations and analyses performed under this contract indicated that:

1. Voice data can be encoded, transmitted, and decoded via the Astrovoice II system operating in conjunction with tracking radar equipment.

2. That speech quality and intelligibility is not seriously degraded by the techniques employed in the Astrovoice II communication system even when the radar beacon on the spacecraft is concurrently interrogated by several tracking radar equipments.

3. The Astrovoice II system can also be used to telemeter data.

It is recommended that an operational one-way Astrovoice II system be constructed and flight tested; that an operational two-way Astrovoice II system be designed, developed, and flight tested; and that signal propagation analyses be conducted relative to application of the Astrovoice II communication system to current and projected space-flight programs.

SECTION II

INTRODUCTION

This report describes work performed in designing and developing the Astrovoice II space communication system. This work was done by Avco Corporation's Research and Advanced Development Division (Avco-RAD) for the National Aeronautics and Space Administration under Contract NASw-586.

The Astrovoice II space communication system is intended for use in transmitting voice or other data from a spacecraft to one or more ground stations via a radar beacon, or transponder, in the spacecraft and ground or ship based tracking radar equipment. This is accomplished without interference with the radar equipment's primary function -- tracking.

Prior to transmission, the information is processed in an encoder to produce a train of pulse position modulated pulses. These pulses, received by the tracking radar equipment, are decoded, or demodulated, to reproduce the information presented for transmission. Voice data can be encoded, transmitted, and decoded into intelligible speech of good quality.

Use of the radar beacon and tracking equipment, which operate at C-band frequencies, enables communication to be maintained even during hypersonic re-entry. Signals transmitted at that frequency, although attenuated by the plasma surrounding the craft during such re-entry, are propagated with sufficient strength to enable their reception by suitable radar equipment.

The initial Astrovoice system was conceived, designed, and developed by Avco-RAD. Subsequently, Avco-RAD submitted a proposal to NASA, Avco document RAD MS-62-53B(L), which presented a program for research and development pertaining to re-entry communication techniques based upon the following-listed specific tasks:

Task I	Encoding/Decoding Equipment Development
Task II	Operational Equipment Analysis
Task III	One-Way Re-entry Communication System Design
Task IV	Propagation Analysis Comparison to Project Mercury Flight Test Data
Task V	Propagation Analysis for Current Manned Spacecraft Programs
Task VI	Two-Way Re-entry Communication System Design.

Contract Number NASw-586, under which the work described in this final report was performed, essentially covered efforts to be expended in accomplishing the first two of these tasks.

Both of these tasks were completed successfully. On this basis, Avco-RAD now recommends that the program be continued through completion of the remaining four tasks.

In addition to this final report, a magnetic tape recording* has been prepared to demonstrate the performance of the breadboard model of the Astrovoice II system as developed under contract NASw-586. The recording, which is being submitted to NASA, presents comparative data indicating the quality and intelligibility of unprocessed speech, speech processed by the Astrovoice II system operating in each of two modes (with, and without radar interrogation of the beacon), and speech processed by a high-gain clipper audio type speech processing system. The selection used for comparison is a recording made by Lt. Col. John Glenn and supplied to Avco-RAD by NASA.

* Identified by Avco-RAD as TIDM-F450-1300.

SECTION III

CONCLUSIONS

Results of the Astrovoice II system design and development program demonstrate that use of a synchronous rectangular audio technique for speech processing is feasible and that speech processed in this manner can then be transmitted after encoding according to a pulse position modulation scheme.

This approach to space communication offers substantial advantages in that high intelligibility, reasonably good quality speech output can be obtained for relatively low pulse rates (on the order of 3700 pulses per second).

Use of the synchronous rectangular audio speech processing system offers a 2 to 1 pulse rate advantage over constant frequency sampling speech processing of similar quality. When using a voice operated transmission (VOX) and squelch circuit in the former system and an advantage of 4 to 3 when such a circuit is not used.

Synchronous rectangular audio processed speech is clearly superior to speech processed by clipper audio systems. Clipper audio processed speech is subject to severe degradation in speech quality and intelligibility due to lost pulses during transmission. In addition synchronous rectangular audio processed speech is free of the annoying inter-word and inter-sentence noise common to speech processed by clipper audio systems.

SECTION IV

RECOMMENDATIONS

Avco-RAD recommends that design and development efforts on the Astrovoice II system using encoder-generated synchronization pulses be extended to the following-listed areas:

1. Development of a phase-lock system to be incorporated in the decoder to improve system accuracy by minimizing the effects of Doppler shift.

2. Incorporation of a suitable voice-operated transmitter (VOX)-squelch circuit in the encoder. Techniques suitable for this application have already been developed in communications practice.

3. Construction and flight-test of an operational one-way Astrovoice II communication system.

4. Design, development, construction, and flight test of a two-way Astrovoice II communication system.

5. Analysis of manned spacecraft re-entry trajectories to obtain signal propagation predictions applicable to employment of Astrovoice II communication systems on current and projected space flights, both of the manned and un-manned, or probe, type.

SECTION V

DISCUSSION

5.1 GENERAL

Section V of this report presents detailed information about the work performed by Avco Corporation's Research and Advanced Development Division (Avco-RAD) in fulfillment of Tasks I and II of Contract Number NASw-586.

This section provides a detailed description of the Astrovoice II system and its components, details the work performed and the methods employed in designing and developing the Astrovoice II system, and presents results of a concurrent and associated human factors engineering study of speech intelligibility.

Section V is arranged as follows:

5.2 Astrovoice II System	A general description of the over-all system.
5.3 Encoder System	A detailed description of the encoder system, including the synchronization and speech processing subsystems.
5.4 Decoder System	A detailed description of the decoder system, including the synchronization and pulse-to-speech demodulating subsystems.
5.5 Radar Equipment	A detailed description of investigations and analyses made on the radar equipment to be used in conjunction with the encoder and decoder systems.
5.6 Speech Intelligibility	A report on results of a human factors engineering study of the speech intelligibility obtained during operation of breadboard models of the Astrovoice II system.
5.7 System Performance	A description of various experiments performed and of the results of those experiments, and of results of a comparative study of three different types of speech processing systems.

Section V indicates various design approaches considered during the program, the criteria for selecting the approaches used, and, in some cases, promising approaches for improving future systems.

In general, figures referred to under each of the main paragraph headings (5.1, 5.2, etc.) of this section follow the last page of text under that heading.

5.2 ASTROVOICE II SYSTEM

The Astrovoice II system is a space communication system designed and developed by the Research and Advanced Development Division of the Avco Corporation (Avco-RAD). The work was performed in accordance with Tasks I and II of Contract No. NASw-586. The system is designed to enable voice transmission from a spacecraft to one or more ground stations via a radar tracking link. The complete communication system, as developed under the current contract, consists essentially of an encoder system in the spacecraft, a decoder system at the ground station, and conventional C-band radar tracking equipment. The tracking equipment includes a beacon and antenna on the spacecraft and a ground-based radar set with its antenna.

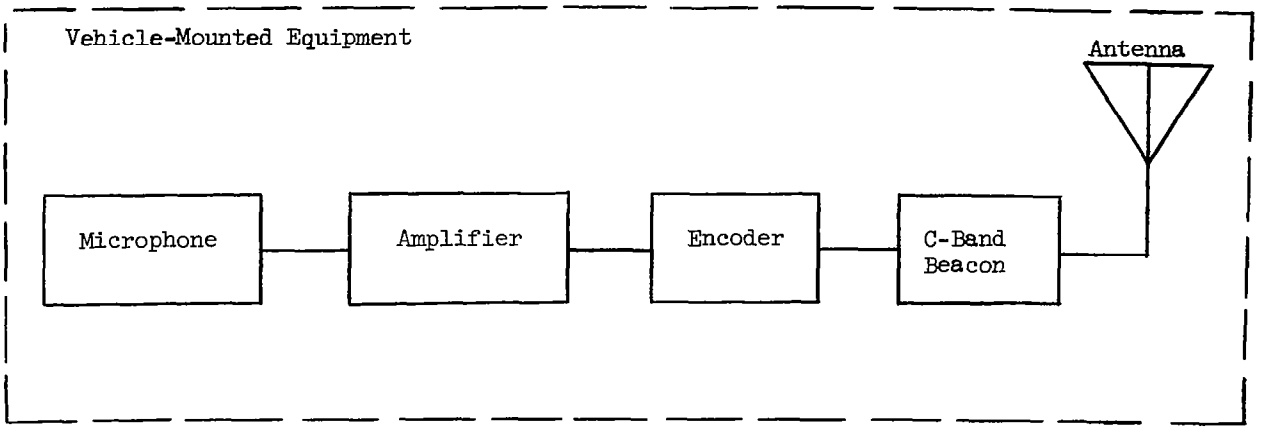
The complete system is identified as the Astrovoice II system to distinguish it from an earlier similar space communication system designed and developed by Avco-RAD.

The Astrovoice II encoder, and decoder systems are shown, in block diagram form, on Figures 5-1, 5-2, and 5-3, respectively.

The encoder and decoder systems are described in paragraphs 5.3 and 5.4, respectively.

Various radar sets, together with their beacons and antennas, are described in paragraph 5.6.

Unless otherwise noted, it will be assumed that the Astrovoice II system will be operating in conjunction with the type FPS-16 radar equipment. This equipment has a pulse rate of 142 pulses per second, as described in paragraph 5.6. The Astrovoice II system is capable of ready adaptation to other pulse rates as indicated in various paragraphs of this report.



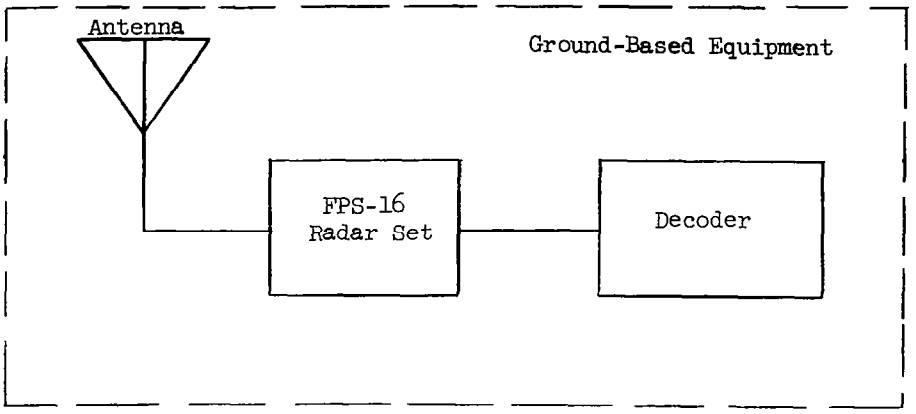


Figure 5-1. Block Diagram, Astrovoice II System

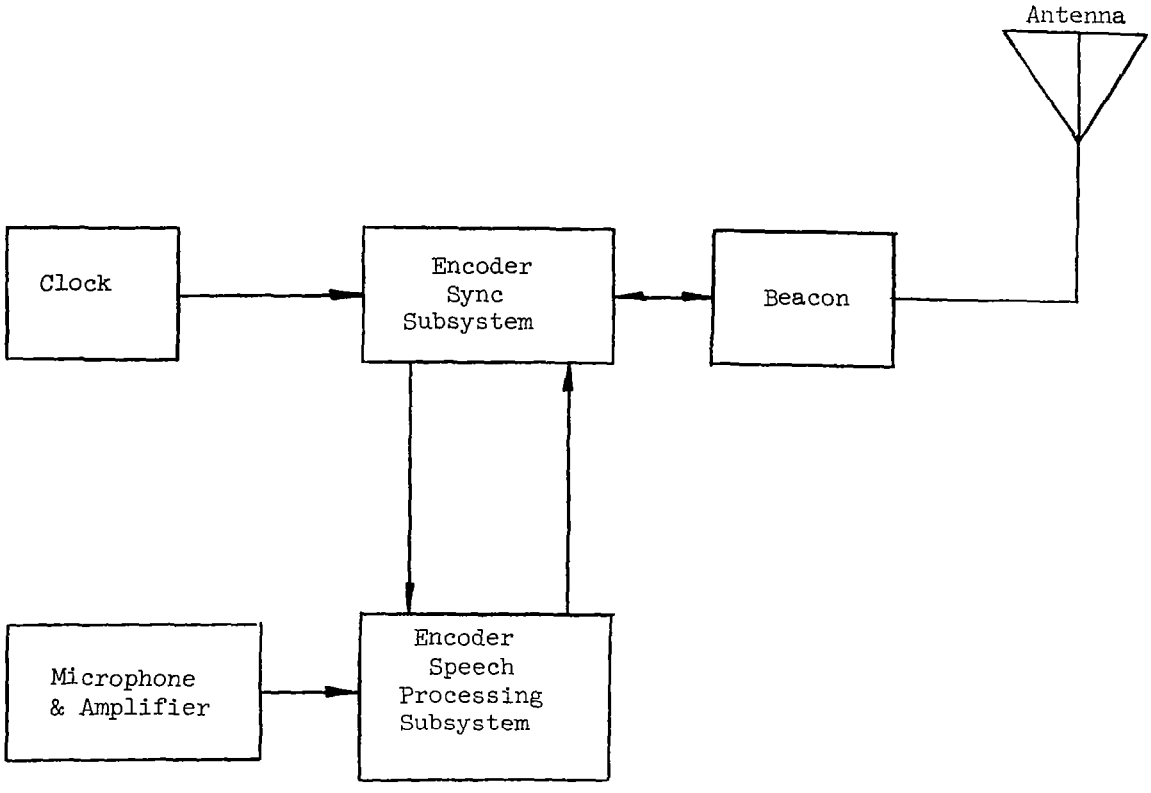


Figure 5-2. Block Diagram, Astrovoice II Encoder System

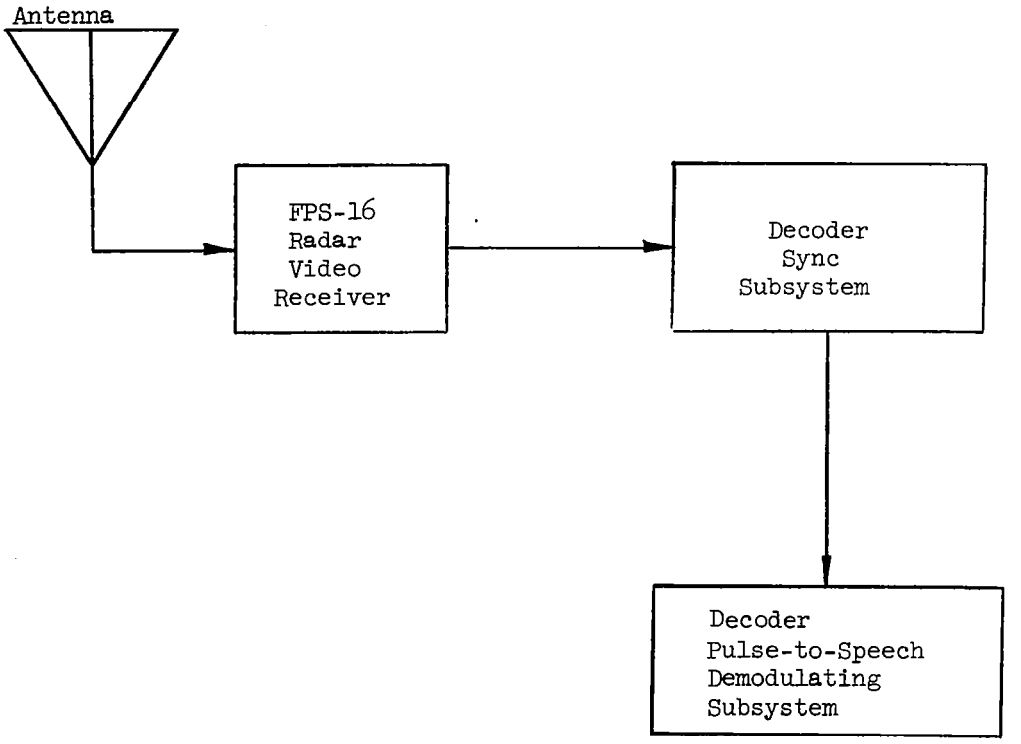


Figure 5-3. Block Diagram, Astrovoice II Decoder System

5.3 ENCODER SYSTEM

The Astrovoice encoder system consists essentially of two subsystems -- the encoder synchronization (sync) subsystem (ESS) and the encoder speech processing subsystem (ESPS). These subsystems are described in detail in paragraphs 5.3.1 and 5.3.2, respectively.

The encoder system, shown in block diagram form on Figure 5-2, receives ground pulses through the C-band beacon and antenna and provides appropriate voice signals to the same beacon and antenna for transmission to one or more ground stations.

In this report the term "ground pulse train" is used to refer to the series of pulses transmitted by the FPS-16 radar set at the rate of 142 pulses per second (pps). The terms "ground pulse" and "ground pulses" are used to refer to one or more of the individual pulses in the ground pulse train.

5.3.1 Encoder Synchronization Subsystem

In combination, the encoder synchronization subsystem (ESS) and the encoder speech processing subsystem (ESPS), together with the microphone and microphone amplifier used to provide voice input to the ESPS, compose the complete Astrovoice II encoder system. The ESS operates in direct conjunction with the C-band beacon as well as with the ESPS.

Major design criteria for the ESS included those imposed by the need to:

Be compatible with the ESPS.

Meet Astrovoice II encoder system synchronization requirements.

Avoid any interference with the tracking functions of the radar equipment.

Among the compatibility factors which influenced ESS design are the following-listed characteristics of the ESPS:

1. A pulse position modulation (PPM) technique is used to transmit information regarding the amplitude of the waveforms used as the analog of speech information.

2. The amplitude information is obtained by sampling the peaks and troughs of the speech analog waveforms. Peaks and troughs are defined as the zero crossings of the differentiated speech analog waveforms.

3. The speech sampling pulses are obtained from the differentiated speech analog waveforms.

4. Pulses at a constant clock rate of 18,176 pulses per second (pps) must be delivered to the ESPS described in paragraph 5.3.2. These

pulses are used to pulse position modulate the speech waveform. The design of the ESPS is such that the amplitude information obtained by the sampling pulses is stored until arrival of a clock pulse. At that time a delayed pulse, called a speech pulse, is transmitted to the beacon. The delay is proportional to the amplitude of the stored pulse. Only the delayed pulse, not the clock pulse, is sent to the beacon.

5. Certain of the clock pulses are transmitted to the decoder system via the beacon and tracking radar equipment. These pulses, which occur at a much slower rate than the normal clock rate, provide the decoder with synchronization reference data and are, therefore, called synchronization (sync) pulses.

In meeting the synchronization needs of the Astrovoice II encoder system the ESS is designed to:

6. Identify all ground train pulses present at the C-band beacon.

7. Insure that all ground train pulses are transmitted without interference by pulses produced by the encoder system.

8. Provide means for synchronizing the decoder system, in both frequency and phase, with the basic pulse rate used by the ESPS in implementing the pulse position modulation techniques.

9. Provide the pulses needed by the ESPS to convert speech analog waveforms to a pulse format for transmission to the decoder via the beacon and tracking radar equipment.

The third major design requirement was the absolute necessity of avoiding interference with the basic tracking functions of the radar equipment with which the Astrovoice II system operates. Two different situations had to be considered:

10. Non-interference with ground pulses from a single tracking radar set.

11. Non-interference with ground pulses from more than one tracking radar set.

A general description of the means of preventing interference with ground pulses follows. More detailed descriptions of the alternative approaches used in designing the ESS to avoid interference with the tracking functions are described in paragraphs 5.3.1.1 and 5.3.1.2. Radar design characteristics related to these situations are described in paragraph 5.6.

If the time interval between two successive pulses received at the beacon is less than 75 microseconds (μsecs), the beacon will lock out, that is, it will not transmit for an interval of 100 μsecs. An analysis of the probability of ground pulse lock-out is given in paragraph 5.3.1.9. Absence of beacon

transmissions will, of course, make tracking difficult and, if such 100 μsec intervals occur too frequently, introduce errors in the tracking data. Speech or sync pulses (or either a speech or sync pulse and a ground pulse), therefore, must not reach the beacon within the 75 μsec interval since their arrival would trigger beacon lock-out. Accordingly, the encoder subsystem is so designed that it can:

12. Know in advance when a ground pulse will arrive.

13. Inhibit speech and sync pulses for a discrete time interval before and after arrival of a ground pulse.

The duration of the pre-ground pulse and post-ground pulse inhibit intervals, generally referred to in this report as the pre-inhibit and post-inhibit intervals, is on the order of 100 μsecs. This provides an adequate safety margin.

The pre-inhibit interval prevents speech or sync pulses from reaching the beacon at a time when they could interfere with a ground pulse arriving or about to arrive at the beacon. In providing the pre-inhibit interval, the ESS design takes advantage of the fact that ground pulse trains from the tracking radar set or sets have a stable pulse rate (142 pps for the FPS-16 radar equipment). Arrival of a ground pulse at the beacon triggers a count-down sequence in the ESS which then provides a pre-inhibit interval prior to the expected arrival time of the next ground pulse in the ground pulse train.

The post-inhibit interval prevents speech or sync pulses from reaching the beacon for at least 75 μsecs (actually, approximately 100 μsecs) after reception of a ground pulse. This arrangement prevents beacon lock out and insures uninterrupted beacon transmission in reply to the ground pulses. The post-inhibit interval is triggered by reception of the ground pulse itself. Such intervals, therefore, follow each ground pulse received at the beacon.

A study of the effects of Doppler shift of the ground pulses indicates that system synchronization will not be adversely affected even by a worst-case shift condition due to motion at a rate of 20,000 miles per hour. In that case the 7,000 μsec period of the ground pulse train will shift no more than ±0.2 μsecs--a shift which the system can easily handle.

5.3.1.1 Non-Interference With Ground Pulses From a Single Tracking Radar Set

Interference with ground pulses in a ground pulse train from a single tracking radar set can be provided by use of a reset type divider, or counter, used to reduce a high clock pulse rate to a lower pulse rate. Such a divider is shown on Figure 5-4. The clock rate of 145,408 pps is first reduced to a rate of 18,176 pps by a divide-by-eight divider (8D) and then reduced to a rate of 142 pps, which is the ground pulse rate, by a divide-by-one hundred twenty-eight divider (128D). This arrangement provides 128 distinct time divisions, each approximately 55 μsecs long, between two successive ground pulses in a

ground pulse train. Reception of a ground pulse sets 128D to a count of $126\frac{1}{2}$. This count is defined as the mid-point in the time interval during which 128D holds a count of 126. In this report the term window is used to refer to the time during which a divider or counter holds a particular count. For example, the 126 window (126W) means the time interval of approximately 55 μsecs from the beginning of the period during which a divider holds a count of 126 until the beginning of the period during which the divider holds a count of 127.

The time interval between the end of the period in which the 128D held a count of 124 (124W) and the beginning of the period during which the counter will hold a count of 127 (127W), about 110 microseconds, is used to provide the required 75-plus μsec pre-inhibit interval for reception of the next expected ground pulse.

To insure that no other pulses reset 128D to the $126\frac{1}{2}$ count, the circuits of the ESS are so arranged that once synchronization has been achieved only those pulses which reach 128D while it holds a count of 126, that is, during the 126 window, can reset the divider and thereby maintain synchronization.

Prior to synchronization, however, the circuit arrangement is such that 128D can be reset to $126\frac{1}{2}$ by any ground pulse received at the beacon. The functions of acquiring synchronization, also referred to as operating in the acquisition mode, and of defining the system as being in synchronization (in sync) are implemented by another divider, the divide-by-sixteen divider (16D). The logical arrangement of 16D in the ESS is shown on Figure 5-5. This divider is triggered, or begins to count, in response to a locally generated synchronization pulse (LGSP). The LGSP occurs approximately at mid-point in the time interval during which 128 holds a count of 127. The divide-by-16 divider is always reset to ZERO when a ground pulse appears in the 126 window of 128D. As long as ground pulses appear during the 126 window of 128D, therefore, the system will remain synchronized.

If 15 consecutive ground pulses are not received and counted during the 126 window, 16D reaches a count of 15 and, by a self-locking feature, retains that count despite reception of additional LGSP's. When locked at a count of 15 in this fashion, the encoder subsystem is defined as being out of synchronization (out of sync) with the ground pulse train. When 16D is locked at a count of 15, any ground pulse received at the beacon terminal resets all the dividers in the ESS (8D to a count of 4, 128D to a count of 126, and 16D to a count of ZERO). The encoder system, when in this condition, is defined as operating, or being, in the acquisition (or out of sync) mode. Once the various dividers have been reset, the system is defined as operating, or being, in sync and the proper pre- and post-inhibit intervals are provided for the ground pulse train to which the system is synchronized.

A major design advantage of this approach to encoder system synchronization is the ease with which the system can be adapted for synchronization with radar transmitters of various pulse rates. All that is needed for such adaptation is selection and use of a suitable clock rate or dividers.

For descriptions of the subsystem logic and electronic circuits used to implement this design approach, see paragraph 5.3.1.7.

5.3.1.2 Non-Interference With Ground Pulses From Multiple Tracking Radar Sets

Alternative approaches can be used to prevent interference with ground pulses in ground pulse trains from more than one tracking radar set. The approaches generally differ from that used to avoid interference with ground pulses from a single tracking radar set. One of the alternative approaches employs a 31-stage shift register type delay line. The register arrangement is shown on Figure 5-6.

The shift pulse rate of the register is 4,544 pps, 32 times that of the ground pulse rate of 142 pps. Ground pulses received at the beacon are loaded serially into the shift register. The delayed output of the register is then used to initiate the pre-inhibit interval. The pre-inhibit interval ends either automatically at the expiration of a pre-determined time interval or with reception of the next ground pulse, according to which event occurs first. Normally, reception of the ground pulse occurs before expiration of the timed interval. The design is such that more than one pulse can be propagated simultaneously through the shift register without interference with other pulses.

Principal characteristics of this type of shift register as used in the ESS are:

1. Shift pulses to the first stage of the shift register occur at 220 μsec intervals. Thus, the resolution of the shift register delay line is 220 μsec since ground pulses are random in time in respect to shift pulses.

2. The delay introduced by the shift register can vary between 6670 and 6890 μsecs. Since ground pulses in a ground pulse train occur at approximately 7042 μsec intervals, pre-inhibit intervals varying from 110 to 330 μsecs can be produced. The average duration of the pre-inhibit interval is 220 μsecs.

3. Reception of the first ground pulse turns the first stage of the register ON. The shift pulse turns OFF those stages which are ON and simultaneously causes a delayed pulse to be transmitted to the next succeeding stage to turn that stage ON. Stages which are OFF do not transmit pulses to succeeding stages. Pulses are transmitted from stage to stage with a delay of 220 μsecs per stage. Up to 32 pulses can be transmitted simultaneously through the shift register.

The shift register can, therefore, provide the pre-inhibit intervals necessary to prevent interference with ground pulses reaching the beacon from more than one ground station. The register described here is designed to work with ground pulse trains having a basic pulse rate of 142 pps or an integral multiple of that rate. Interference with ground pulses occurring at other rates than 142 pps can be prevented by using a different number of register stages, or a different shift pulse rate, or some combination of these modifications.

For descriptions of the subsystem logic and electronic circuits used to implement this design approach, see paragraph 5.3.1.8.

5.3.1.3 Formation of Synchronization and Modulation Reference Pulses

The Astrovoice II encoder employs a pulse position modulation technique for transmittal of speech information. Only the modulated pulses, not the constant frequency pulses used as reference pulses in implementing the pulse position modulation (PPM) technique, are transmitted. The modulated pulses are generally referred to in this report as speech pulses.

The Astrovoice II decoder, however, requires some type of modulation reference, or sync, pulses to enable demodulation of the pulse position modulated pulses to yield speech information.

The sync pulses are transmitted at a rate much slower than the speech pulse rate. The decoder maintains synchronization by reference to a stable internal clock. This clock operates at the same pulse rate as the encoder clock. The decoder clock is synchronized with the encoder clock in both frequency and phase by the sync, or modulation reference, pulses transmitted by the encoder.

Although the sync pulses contain no speech information, they are essential to the demodulation process. Accordingly, they have a higher priority than speech pulses in transmission from the beacon. Provision has, therefore, been made in the design of the encoder for a pre-inhibit interval designed to insure that speech pulses do not interfere with transmission of the sync pulses. Although sync pulses have a higher priority than speech pulses, they must not, however, interfere with the ground pulses received at the beacon.

5.3.1.4 Sources of Sync Pulses

Sync pulses can be derived either from ground pulses or from the encoder itself, as follows:

5.3.1.4.1 Sync Pulses from Ground Pulse Source

If the beacon is within range of a tracking station and the tracking equipment is working properly, ground pulses will be available at the beacon. The ground pulses are an excellent source of sync pulses since they are protected from interference by an appropriate pre-ground pulse inhibit interval, as described in paragraph 5.3.1 and they have an almost constant pulse rate with a period of approximately 7,000 μsecs (plus or minus 0.2 μsecs if the effect of Doppler shift is included).

Incorporation of this approach in the basic clock rate divider system is shown on Figure 5-7. During the time interval between successive ground pulses the 18,176 pps reference pulses will be phase synchronized with the ground pulse. Since the decoder and encoder each have both a clock providing pulses at a 145,408 pps rate and a divide-by-eight divider (8D) which is reset to a count of 4 by the ground pulses, the decoder can reproduce the reference pulses at the same rate as they are produced by the encoder -- 18,176 pps. These pulses can then be used by the decoder in the demodulation process.

By using the ground pulses to synchronize the encoder reference pulses a resolution of approximately 7 μsecs (the inter-pulse spacing of the clock) can be obtained. Thus the 18,176 pps encoder reference pulse train will be in phase within 7 μsecs for the basic 55 μsec reference pulse period.

The same situation exists in the decoder. The phase difference between the encoder and decoder 18,176 pps reference pulse trains, therefore, can only vary from a minimum of 0 μsecs to a maximum of 14 μsecs. Even this slight phase difference can be eliminated by incorporation of appropriate automatic frequency control features in the encoder and decoder clocks.

If ground pulses from more than one tracking radar pulse train are to be received at the beacon, provision can be made for the encoder to identify by a special 'tag' the pulse train to which it is synchronized. This avoids the possibility of the encoder and decoder being sychronized with ground pulses from different ground pulse trains.

5.3.1.4.2 Sync Pulses from Encoder Source

The encoder can provide its own sync pulses and transmit them to the beacon. Generation of such sync pulses can be completely independent of the encoder sync functions relative to generation of sync pulses derived from a ground pulse train.

The method used for encoder generation of sync pulses is flexible. Certain pulses are selected from the train of modulation reference pulses entering the speech processing subsystem. The selected pulses, which occur at a rate much slower than the average rate of the speech pulses, are then transmitted as sync pulses to the beacon at a constant rate. These sync pulses are used to provide the decoder with the timing information necessary for demodulating the speech pulses.

Implementation of this system of generating sync pulses requires incorporation of two basic logic components in the encoder sync subsystem. One component is used to provide the pre-ground pulse inhibit interval necessary to prevent interference with the ground pulse trains by the speech or sync pulses. The second logic component provides modulation reference pulses to the encoder speech processing subsystem and selects certain pulses from the modulation reference pulses. The selected pulses serve as sync pulses and, when considered as a series of pulses, they constitute a sync pulse train.

A divider is used to select the sync pulses. The logic arrangement employed for the divider, which can consist of the divide-by-8 and divide-by-128 dividers described previously, is shown on Figure 5-8. A flip-flop (FF), or bi-stable multivibrator, is used in conjunction with the divider to provide the pre-ground pulse inhibit intervals needed for ground pulse train protection. When the FF is set to the ONE state, the FF output is applied to an inhibit gate to prevent transmission of modulation reference pulses. The free running clock, shown on Figure 5-8, is used to provide the encoder-generated sync pulses. It may be either the same clock as that used in the ground pulse train protection logic arrangement shown on Figure 5-4 or it

may be a completely different and independent clock. Provision is made in the selection of the divider to assure that the sync pulses are produced at a rate different from the ground pulse rate. This is done to avoid possible ambiguity when both sync and ground pulses appear at the input to the decoder.

Although operation of the encoder in generating sync pulses will be unaffected by the Doppler shift which will change the sync pulse period by the time the sync pulses actually reach the decoder, provision must be made in the design of the decoder to compensate for the shift through incorporation of appropriate frequency and phase control circuits in the decoder.

5.3.1.5 Elimination of Noise Interference Resulting From Ground Pulses

Provision is made in the encoder designs for elimination of noise interference resulting from ground pulses. This is accomplished in the encoder by incorporating suitable means for tagging the noise pulses resulting from ground pulses and in the decoder by incorporating suitable means for identifying and then eliminating the noise pulses.

Two circumstances combine to produce the noise pulses. First, ground pulses normally occur at random times in relation to occurrence of modulation reference pulses (MRP's). Second, in the PPM technique employed in the Astrovoice II system, the modulation reference, or clock, pulse which occurs immediately following a peak/trough (P/T) pulse is time-modulated, or delayed, for a period of time proportionate to the amplitude of the speech waveform at the time the P/T pulse occurred. The actual delay may vary from 0 to 14 microseconds. Any ground pulse occurring during this delay period, or modulation interval (MI) as it is generally termed, would then be transmitted as a noise pulse of random amplitude. Presence of this noise pulse in the demodulated output of the decoder would produce noise interference.

Means to prevent such noise interference have been provided, however. The encoder logic has been designed to use the modulation intervals as gates, or windows, during which the encoder senses whether or not a ground pulse is present. Whenever such sampling indicates that a ground pulse is present during the modulation interval, the encoder automatically produces a delayed, or tag, pulse and temporarily inhibits transmission of sync and speech pulses. A timing diagram showing the relationship between the ground pulses and the delay intervals is shown on Figure 5-9. The logic arrangement used to generate the tag pulse and to inhibit the sync and speech pulses is shown on Figure 5-10. The tag pulse is used by the decoder to identify existence of a random amplitude noise pulse in the speech pulse train. Suitable means are then employed to eliminate the noise pulse and, therefore, the interference which it would produce if it were to appear in the demodulated output of the decoder.

5.3.1.6 Alternative Approaches to Encoder Sync Subsystem Logic

As noted previously (paragraphs 5.3.1.1 and 5.3.1.2), the encoder sync subsystem can be designed to prevent interference with ground pulses from a single tracking radar set or, alternatively, to prevent interference with ground pulses from more than one tracking radar set. Details of the encoder

sync subsystem logic used to implement these alternative design approaches are presented in paragraphs 5.3.1.7 and 5.3.1.8, respectively.

5.3.1.7 Encoder Sync Subsystem Logic and Components (Single Ground Pulse Train)

5.3.1.7.1 General

Results of tests of an encoder sync subsystem designed to prevent interference with ground pulses from a single tracking radar set indicate conclusively that the logic system described here and shown in block diagram form on Figure 5-11 can be successfully implemented in an operational Astrovoice system. Binary solid-state (transistor/diode) dividers and standard-type solid-state (transistor/diode) AND, OR, and INHIBIT logic blocks, or modules, were used in constructing the subsystem. Logic operation was thoroughly tested, not only when operating the encoder sync subsystem alone, but also when operating the subsystem in conjunction with both the encoder speech processing subsystem and the complete decoder system.

It should be noted that the block diagram of this subsystem, shown on Figure 5-11, represents an expansion and, to some extent, a revision of the diagrams shown on Figures 5-4, 5-5, 5-7, 5-8, and 5-10.

5.3.1.7.2 Subsystem Functional Requirements

Analysis of design requirements for an encoder sync subsystem capable of transmitting voice data via a radar beacon without interfering with ground pulses arriving from a single tracking radar set indicated that the subsystem must be capable of performing the following-listed functions.

1. Detecting sequential ground pulses. These pulses are normally time-spaced approximately 7,000 μsecs apart.

2. Providing pre-inhibit intervals adequate to prevent the communication system from interfering with ground pulses reaching the beacon from the tracking radar set.

3. Identifying, or tagging, ground pulses which could cause noise interference through their appearance in the time interval assigned for formation and transmission of pulse position modulated speech pulses.

4. Providing serial synchronization, or sync, pulses time-spaced approximately 7055 μsecs apart.

5. Providing pre-inhibit intervals adequate to prevent sync pulses from reaching the beacon at such times that their transmission might provide spurious returns to the tracking radar set.

6. Transmitting all speech pulses to the beacon.

7. Providing adequate post-inhibit intervals for all sync and speech pulses appearing at the beacon closely following appearance of ground, sync, or speech pulses at the beacon.

8. Transmitting pulses according to the following-listed order of priority to assure that speech pulses do not inhibit sync or ground pulses even during continuous encoder operation.

   a. Ground pulses.

   b. Sync pulses.

   c. Speech pulses.

5.3.1.7.3. Component Functional Requirements

The following list identifies the essential components required to mechanize the encoder sync subsystem logic and indicates their principal functions.

1. A clock which provides basic timing data.

2. A divide-by-8 divider (8D) used to provide modulation reference pulses (MRP's) at a rate of approximately 18,176 pps.

3. A divide-by-128 divider (128D) to enable pre-inhibit and post-inhibit intervals to be provided for every ground pulse and to provide synchronization pulses for the subsystem.

4. A divide-by-16 divider (16D) and associated logic circuits to gate ground pulses entering the subsystem.

5. A pre-inhibit flip-flop (PREI) used in conjunction with 128D to provide pre-inhibit intervals.

6. A monostable multivibrator to provide post-inhibit intervals for every pulse transmitted to the beacon by either the encoder system or the radar tracking set.

7. An element to provide locally generated sync pulses (LGSP's).

8. An element to prevent MRP's from entering the encoder speech processing subsystem during the pre- and post-inhibit intervals.

5.3.1.7.4 Component Operation

The major components of the encoder sync subsystem designed to prevent interference with ground pulses from one tracking radar set operate as follows. Interconnections between these components are shown on Figure 5-11. In the interest of conserving design effort, certain of the major components (crystal-controlled oscillator, regenerative clipper, clock pulse generator, and the

divide-by-eight and divide-by-128 dividers) described here have been so designed that they can be used alternatively in either the encoder or decoder sync subsystem with only slight modifications.

5.3.1.7.4.1 Clock

The clock is basically a crystal-controlled oscillator (CO) whose frequency of 145,408 pps is 1,042 times the rate of the ground pulses (142 pps). The clock provides basic timing information for the system. For a circuit description and schematic diagram, see paragraph 5.3.1.7.6.1 and Figure 5-29, respectively.

5.3.1.7.4.2 Regenerative Clipper

The regenerative clipper (RC) produces square wave output signals in response to sinusoidal input signals received from the crystal-controlled oscillator. For a circuit description and schematic diagram, see paragraph 5.3.1.7.6.2 and Figure 5-30, respectively.

5.3.1.7.4.3 Divide-by-Eight Divider

The divide-by-eight divider (8D) produces output pulses at a rate of 18,176 pps to trigger the clock pulse generator. Both ground phase (Gϕ) and audio phase (Aϕ) pulses are produced. Gϕ pulses are produced when 8D begins to hold a count of 4. They are in phase with the ground pulses used in synchronizing the encoder sync subsystem. Aϕ pulses are produced when 8D begins to hold a count of 8. 8D is reset by ground pulses via a counter reset circuit. The divider consists essentially of three bistable multivibrators, or binary dividers, interconnected logically as shown on Figure 5-12. The circuit of one stage of the divider is shown schematically on Figure 5-13. The multivibrators used in 8D are the triggered type A described in paragraph 5.3.1.7.6.5 and shown schematically on Figure 5-33.

5.3.1.7.4.4 Clock Pulse Generator

The clock pulse generator (CPG) receives Gϕ and Aϕ pulses from 8D and provides Gϕ pulses to both the Gϕ 127 AND gate (Gϕ 127) and the pre-inhibit flip-flop (PREI), Aϕ 1 pulses to the modulation reference pulse (MRP) AND gate and Aϕ 2 pulses to trigger 128D. The clock pulse generator is composed essentially of two monostable multivibrators. The multivibrators are similar to the type described in paragraph 5.3.1.7.6.3. For a circuit description and schematic diagram, see paragraph 5.3.1.7.6.3 and Figure 5-31, respectively.

5.3.1.7.4.5 Divide-by-128 Divider

The divide-by-128 divider (128D) receives Aϕ 2 input pulses from the clock pulse generator. It provides output pulses during the 124, 126, and 127 windows (124W, 126W, 127W--that is, during the time (approximately 55 μsecs)

it holds a count of 124, 126, or 127). The counter is reset to a point midway through the 126 window by sync pulses from a counter reset circuit. The point to which it is reset is generally referred to as the $126\frac{1}{2}$ window ($126\frac{1}{2}$W). The 124W, 126W, and 127W output pulses are used as follows:

124W and GØ pulses set the pre-inhibit flip-flop (PREI).

126W and ground pulses synchronize the encoder sync subsystem via a reset OR gate and counter reset circuit which provide the sync pulses used to reset 8D, 128D, and the divide-by-16 divider (16D).

127W and GØ pulses reset the pre-inhibit flip-flop and serve as locally generated sync pulses (LGSP's).

The divider consists essentially of seven serial bistable multivibrators, or binary dividers, interconnected logically as shown on Figure 5-14. The circuit of one stage of the divider is shown schematically on Figure 5-15. Negative outputs are used, thus 127_{10} is represented by a 0000000_2 output instead of by a 1111111_2 output. The binary output corresponding to each of the decimally-designated windows of concern is:

Decimal	Binary
127	0000000
126	0000001
124	0000011

The multivibrators used in 128D are the triggered type B described in paragraph 5.3.1.7.6.6 and shown schematically on Figure 5-34.

5.3.1.7.4.6 Divide-by-16 Divider

The divide-by-16 divider (16D) receives input pulses from the divide-by-16 lock-up circuit (16DLU). 16D is always counting LGSP pulses, except when self-locked. But when the ESS is in sync, 16D is reset to ZERO immediately before every count of one. When 16D holds a count of 15 it provides a ZERO output signal to the 15 window circuit (15W). This signal is used in the reset OR and counter reset circuits to gate ground pulses. 16DLU and 15W operate in conjunction with 16D to provide a self-locking feature. Whenever 16D holds a count of 15, 15W operates through 16DLU to inhibit further counting by 16D, thereby locking 16D at the count of 15. 16D is reset by sync pulses from the counter reset circuit. The divider is composed of four serial bistable multivibrators, or binary dividers, interconnected logically as shown on Figure 5-16. As shown on the schematic diagram of one stage of the divider, Figure 5-17, set and reset pulses are applied to the transistor bases. Negative outputs are used, thus 15_{10} is represented by a 0000_2 output and 0_{10} is represented by a 1111_2 output instead of by 1111_2 and 0000_2 outputs, respectively.

5.3.1.7.4.7 Fifteen-Window

The 15 window circuit (15W) provides a ONE output signal to the divide-by-16 lock-up circuit and to the reset OR gate in response to a ZERO level input signal from 16D. The input signal occurs when 16D holds a count of 15. 15W is used, as noted previously, with 16D and 16DLU to provide 16D with self-locking capabilities. Basically 15W consists of a transistor inverter and a diode. The circuit is shown schematically on Figure 5-18.

5.3.1.7.4.8 Divide-by-16 Lock-up

The divide-by-16 lock-up circuit (16DLU) receives input signals from both 15W and the GØ 127 AND gate. 16DLU is used, as noted previously, with 15W and 16D to provide 16D with self-locking capabilities. The circuit, shown in schematic diagram form on Figure 5-19, consists essentially of a diode and a transistor arranged in an inhibit gate configuration. Locally generated sync pulses (LGSP's) coming to 16DLU from the GØ AND gate are shunted to ground by the transistor whenever the 15W signal is present at 16DLU (that is, whenever 16D holds a count of 15). As a result, the LGSP's cannot enter 16D and further counting by 16D is inhibited.

5.3.1.7.4.9 Reset OR Circuit

The reset OR circuit enables the counter reset circuit whenever either or both of the following-listed input signals are present:

A 126W signal (from 128D).

A 15W signal.

The circuit, shown in schematic diagram form on Figure 5-20, is that of a two-transistor OR gate similar to that described in paragraph 5.3.1.7.6.9 and shown schematically on Figure 5-37.

5.3.1.7.4.10 Counter Reset

The counter reset circuit receives input signals from the ground pulse detector and the reset OR circuit. It provides output signals in the form of sync pulses. These pulses are used to reset 8D, 128D, and 16D. The circuit, shown schematically on Figure 5-21, consists essentially of an input stage followed by three pulse inverters.

5.3.1.7.4.11 GØ 127 AND Gate

The GØ 127 AND gate (GØ 127) receives input signals from 127W (from 128D) and from the clock pulse generator (GØ pulses). When both of these signals are present GØ 127 provides locally generated sync pulses (LGSP's). These pulses are used in the encoder sync subsystem for internal logic and timing purposes.

They are transmitted to the beacon when operating in the acquisition mode. The circuit, shown schematically on Figure 5-22, is similar to the AND gate circuit described in paragraph 5.3.1.7.6.8 and shown in schematic diagram form on Figure 5-36.

5.3.1.7.4.12 Pre-Inhibit Flip-Flop

The pre-inhibit flip-flop (PREI) is used to provide the pre-ground pulse reception interval necessary to prevent sync or speech pulses from interfering with the ground pulses. PREI is set by GØ pulses when 128D holds a count of 124. Its output signal is applied to the modulation reference pulse AND gate (MRP AND) to prevent AØ pulses from entering the encoder speech processing subsystem. PREI is reset by the output of GØ 127. The circuit, shown in schematic diagram form on Figure 5-23, is essentially similar to that of the set-reset type bistable multivibrator described in paragraph 5.3.1.7.6.4 and shown schematically on Figure 5-32.

5.3.1.7.4.13 Modulation Reference Pulse AND Gate

The modulation reference pulse AND gate (MRP AND) is used to control entry of AØ 1 pulses into the encoder speech processing subsystem. The AØ 1 pulses can enter the speech processing subsystem except when either the pre-inhibit flip-flop (PREI) or the post-inhibit monostable multivibrator are set. The output signals from PREI and POI are inverted to allow use of an AND gate configuration. The MRP AND circuit is shown schematically on Figure 5-24. It is a conventional AND gate similar to that described in paragraph 5.3.1.7.6.8 and shown schematically on Figure 5-36. The latter figure shows the inverter transistors.

5.3.1.7.4.14 Post-Inhibit Monostable Multivibrator

The post-inhibit monostable multivibrator (POI) is used to provide the post-inhibit interval necessary to insure that ground, sync, and speech pulses do not occur on the beacon line less than 100 μsecs apart. Thus no information can be lost due to beacon lock-out. POI is triggered by each pulse appearing on the beacon line, regardless of whether the pulse comes from the beacon or from the encoder sync subsystem. The output signal from POI is applied to MRP AND to control entry of AØ pulses into the sync subsystem. It is reset automatically at the end of 100 μsecs, thereby ending the post-inhibit interval. The circuit, shown schematically on Figure 5-25, is basically the same as that of the monostable multivibrator described in paragraph 5.3.1.7.6.7 and shown schematically on Figure 5-35.

5.3.1.7.4.15 Ground Pulse Detector

The ground pulse detector (GPD) receives input signals from the beacon (ground pulses) and from the beacon driver (sync and speech pulses). It provides an

output signal to the counter reset circuit. Sync and speech pulses are self-inhibited whenever present at the GPD inputs. The GPD output signal is, therefore, produced in response to the ground pulse only. The GPD circuit is shown schematically on Figure 5-26. The circuit is essentially the same as that of the inhibit gate described in paragraph 5.3.1.7.6.10 and shown schematically on Figure 5-38.

5.3.1.7.4.16 Beacon Driver

The beacon driver (BD) provides means for impedance matching between the encoder sync subsystem and the beacon. Input signals to the driver are either locally generated sync pulses (LGSP's) from GØ 127 or speech pulses from the encoder speech processing subsystem. BD provides output signals (sync or speech pulses) to the beacon, to the ground pulse detector (GPD) and to the post-inhibit monostable multivibrator (POI). The BD circuit is shown schematically on Figure 5-27. The circuit is essentially the same as that described in paragraph 5.3.1.7.6.12 and shown schematically on Figure 5-40. The principal difference is that the latter figure does not show the input transistors and associated components and circuits.

5.3.1.7.5 Logic States

Descriptions of the various states of the encoder sync subsystem logic and of the state of individual components at each state of the encoder sync subsystem logic follow. The logic flow diagram shown on Figure 5-28 indicates basic interrelationships between the various logic states.

STATE I — No ground pulses being received at the encoder

a. The pre-inhibit flip-flop (PREI) is set to a ONE state by a ground phase pulse (GØ) from the clock pulse generator (CPG) when the divide-by-one hundred twenty-eight divider (128D) holds a count of 124. PREI is reset, or cleared, to a ZERO state by the output of the GØ 127 AND gate (GØ 127).

b. The divide-by-sixteen divider (16D) is locked at a count of 15.

c. The GØ 127 and the modulated audio phase 1 (AØ 1) signals (speech pulses) are being transmitted to the beacon. The AØ 1 signals serve as modulation reference pulses and they are, accordingly, transmitted to the encoder speech processing subsystem. The GØ 127 and speech pulse outputs also trigger the post-inhibit one-shot multivibrator (POI).

STATE II — A ground pulse arrives

a. The divide-by-eight divider (8D) is set to a count of four and 128D is set to a count of 126.

b. Arrival of the ground pulse sets 16D to a ZERO count and GØ 127 produces a count of ONE.

NOTE: Both a. and b. occur when a ground pulse appears either: 1) during the 126 window (that is when 128D holds a count of 126) or 2) following STATE I.

c. PREI is set to a ONE state when 128D holds a count of 124. PREI is reset to the ZERO state when 128D holds a count of 127.

d. The ground pulse and speech pulse signals are being transmitted. These signals also trigger POI.

NOTE: The encoder system is then, by definition, synchronized, or 'in sync'.

STATE III-1 From one to fourteen consecutive ground pulses, inclusive, are absent from a ground pulse train while 128D holds a count of 126

a. 16D counts the LGSP's.

b. PREI is set to a ONE state by pulses from the CPG when 128D holds a count of 124. PREI is reset to the ZERO state by the output of GØ 127.

c. Only the speech pulse signal is being transmitted. This signal also triggers POI.

STATE III-2 The ground pulse arrives while 128D holds a count of 126 and before 16D reaches a count of 15

a. 16D is reset to a count of ZERO.

b. The encoder sync subsystem reverts automatically to STATE II.

STATE III-3 No ground pulses are received immediately (within approximately 7,000 μsecs) after 16D reaches a count of 15

a. 16D is locked at a count of 15.

b. The encoder sync subsystem automatically reverts to STATE I.

5.3.1.7.6 Basic Encoder/Decoder Sync Subsystem Circuits

Descriptions of the basic electronic circuits used to perform logic and timing

functions in the encoder and decoder sync subsystems follow. Applications for these circuits in the encoder and decoder sync subsystems are described in paragraphs 5.3.1.7, 5.3.1.8, 5.3.2.1, 5.4.1.4, and 5.4.2.1.

5.3.1.7.6.1 Crystal-Controlled Oscillator

The crystal-controlled oscillator circuit is shown in schematic diagram form on Figure 5-29. The output frequency is 145,408 pulses per second. This frequency is maintained within 0.01% by a feedback loop which employs a series resonant 145,408 pps crystal. A tank circuit is used in the collector output to center the alternating current (AC) output around 3.8 volts. This voltage is then applied to the buffer amplifier stage which provides a 5-volt peak-to-peak (p-t-p) sinusoidal output signal. The output impedance is approximately 200 ohms.

5.3.1.7.6.2 Regenerative Clipper

The regenerative clipper circuit is shown in schematic diagram form on Figure 5-30. A conventional Schmitt-type trigger circuit is used to produce a square wave output signal in response to a sinusoidal input signal. Input is from the crystal-controlled oscillator. Output is to the divide-by-eight divider.

5.3.1.7.6.3 Clock Pulse Generator

The clock pulse generator circuit is shown schematically on Figure 5-31. The clock pulse generator is, essentially, a monostable multivibrator. The square wave output pulse width is approximately 1 μsec. It receives input pulses and provides output pulses in the encoder and decoder sync subsystems as follows:

Input	From	Sync Subsystem
Audio Phase (AØ)	8D	Encoder & Decoder
Ground Phase (GØ)	8D	Encoder & Decoder
Output	**To**	**Sync Subsystem**
Audio Phase 1 (AØ 1)	MRP Gate 128D	Encoder Decoder
Audio Phase 2 (AØ 2)	Mono 128D	Encoder Decoder
Ground Phase (GØ)	GØ 127 PREI LGMP	Encoder Encoder Decoder

5.3.1.7.6.4 Bistable Multivibrator, Set-Reset Type

The set-reset type bistable multivibrator is a standard flip-flop. A typical circuit is shown in schematic diagram form on Figure 5-32. Set and reset voltages are applied to the bases of the transistors. Output signals are taken from the opposite collectors. By definition, a set input applied at A produces a ONE output signal at C and a reset input applied at B produces a ZERO output signal at C.

5.3.1.7.6.5 Triggered Bistable Multivibrator, Type A

The triggered bistable multivibrator, type A, circuit is shown schematically on Figure 5-33. It is essentially a binary divider operating on a square wave input signal. It is triggered and reset by pulses applied to the collector of the reset transistor. The reset pulse width is approximately 2 μsecs.

5.3.1.7.6.6 Triggered Bistable Multivibrator, Type B

The triggered bistable multivibrator, type B, circuit is shown schematically on Figure 5-34. It is essentially a binary divider. It is triggered by pulses applied through steering circuits to the bases of the transistors. These pulses are normally received from the collector circuits of a preceding similar multivibrator. The output signal is obtained from the transistor collector circuits through a diode. The divider is reset by a drop in the collector voltages.

5.3.1.7.6.7 Monostable Multivibrator

A typical monostable multivibrator circuit is shown in schematic diagram form on Figure 5-35. The circuit is designed to employ two different voltage levels. This arrangement provides a relatively simple method of:

1. Improving timing accuracy by allowing the capacitor, C, to be discharging on the steep portion of the exponential curve when the multivibrator returns to the stable state.

2. Improving recovery time while also saving power by enabling use of a relatively low value resistor in the low voltage power supply. If only a high voltage power supply were used, the resistance value would have to be considerably greater.

The multivibrator period is approximately:

$$T \approx (47 \times 10^3)\ (C)\ (\ln 4/3)$$

Where:

T = multivibrator period.

C = capacitance

ln = natural logarithm.

5.3.1.7.6.8 AND Gate

A typical AND gate circuit is shown in schematic diagram form on Figure 5-36. The two input transistors actually perform an inverting function. They can be considered as corresponding to the transistors in a monostable multivibrator or standard flip-flop, depending upon the circuit arrangement used. Be definition, input signals must be present at both A and B to produce an output signal at C.

5.3.1.7.6.9 OR Gate

A typical OR gate circuit is shown in schematic diagram form on Figure 5-37. A positive-going input signal applied to either A or B or to both A and B causes the voltage at C to drop to ground level.

5.3.1.7.6.10 Inhibit Gate

A typical inhibit gate circuit is shown schematically on Figure 5-38. An input signal at B inhibits an input signal applied at A, thereby preventing an output signal from appearing at C. When input A is not inhibited the output at C is the inverse of the input at A.

5.3.1.7.6.11 Inverter

A typical inverter circuit is shown in schematic diagram form on Figure 5-39. The output signal at B is the inverse of the input signal applied at A.

5.3.1.7.6.12 Beacon Driver

The beacon driver circuit is shown in schematic diagram form on Figure 5-40. The circuit essentially performs an impedance matching function, thereby serving as an impedance transformer. It is used to drive a 47 ohm load -- the C-band beacon. By suitable component selection the beacon driver circuit can be readily modified to drive loads of other impedance values.

5.3.1.8 Encoder Sync Subsystem Logic and Components (Multiple Ground Pulse Trains)

5.3.1.8.1 General

The logic and components of an encoder sync subsystem designed to prevent interference with ground pulses from multiple tracking radar sets are described in the following paragraphs (paragraphs 5.3.1.8.2 through 5.3.1.8.4). The block diagram of the subsystem is shown on Figure 5-41. This diagram represents an expansion and, to some extent, a revision of the diagrams shown on Figures 5-6, 5-8, and 5-10.

To assure adequate evaluation of the feasibility of such a sync subsystem, the initial 'paper' design effort was extended to definition of actual logic elements and their detailed functions and to selection of the electronic circuits needed to mechanize the logic. In addition, individual components or circuits were either purchased or constructed in breadboard model form and then tested. A complete model of the over-all encoder sync subsystem of the type described here was constructed and tested with successful results.

5.3.1.8.2 Subsystem Functional Requirements

Analysis of design requirements for an encoder sync subsystem capable of transmitting voice data via radar beacon without interfering with ground pulses arriving at the beacon from more than one tracking radar set indicated that the basic subsystem functional requirements were essentially the same as those for a sync subsystem capable of preventing interference with ground pulses reaching the beacon from a single tracking radar set. These requirements are described in paragraph 5.3.1.7.2. However, the additional capability of preventing interference with ground pulses in ground pulse trains not from one but from multiple tracking radar sets has to be included.

5.3.1.8.3 Component Functional Requirements

The following list identifies the essential components required to mechanize the encoder sync subsystem and indicates their principal functions.

1. A clock which provides basic timing data.

2. A divide-by-1,032 divider (1032D) used to provide sync pulses at a rate of approximately 141 pps and to provide a pre-inhibit interval of approximately 110 μsecs.

3. A divide-by-32 divider (32D) used in series with a 31-element shift register to enable a pre-inhibit interval of from 110 to 330 μsecs to be provided for every ground pulse. The ground pulses may occur in ground pulse trains from several as well as from only one tracking radar set. Typically, they occur at a rate of 142 pps.

4. A flip-flop and a monostable multivibrator used in combination not only to provide tag pulses for any ground pulse received during the modulation interval (14 μsec, maximum) but also to provide a pre-inhibit interval for such tag pulses.

5. An element to provide modulation reference pulses to the encoder speech processing subsystem as well as means to suppress such pulses during the pre- and post-inhibit intervals.

6. A monostable multivibrator to provide post-inhibit intervals for every pulse transmitted to the beacon by either the encoder system or the radar tracking sets.

5.3.1.8.4 Component Operation

The major components of the encoder sync subsystem designed to prevent interference with ground pulses from multiple tracking radar sets operate as follows. The components referred to here are shown on Figure 5-41.

5.3.1.8.4.1 Clock

The clock is basically a crystal-controlled stable oscillator whose frequency of 145,408 pps is 1,042 times the rate of the ground pulses (142 pps). The clock provides basic timing information for the subsystem.

5.3.1.8.4.2 Divide-by-1032 Divider

The divide-by-1032 divider (1032D) is a free running divider which receives input pulses directly from the clock. The divider consists essentially of eleven core/transistor logic elements (CTL's 1 through 11, inclusive). The output pulses from the divider serve as sync pulses. Three core/transistor logic elements (CTL's 12-14) and two core/transistor register stages (CTR's 32 and 33) are used to provide pre-inhibit intervals for the sync pulses. The period (approximately 7,097.2 μsecs) of the 140.9 pps sync pulses is approximately 55 μsecs longer than the 7,042 μsec period of the 142 pps ground pulses.

5.3.1.8.4.3 Divide-by-32 Divider

The divide-by-32 divider (32D) is a five-stage divider consisting essentially of five of the core/transistor logic elements (CTL's 1 through 5, inclusive) also used in 1032D. 32D is used to divide the basic clock frequency of 145,408 pps by 32 to produce pulses at a rate of 4,544. These pulses, which have a period of approximately 220 μsecs, are applied through three core/transistor driver elements (CTD's 1 through 3, inclusive) to a 31-stage shift register.

5.3.1.8.4.4 Thirty-one Stage Shift Register

The 31-stage shift register is a delay-line type shift register which consists of 31 core/transistor register stages (CTR's 1 through 31, inclusive)

used in conjunction with three core/transistor logic elements (CTL's 15, 16, 17). The register contents are shifted every 220 μsecs in response to the output pulses from 32D. Ground pulses entering the register from the beacon initiate the shifting operation. Use of the shift register enables delays of from 6670 to 6890 μsecs to be produced. The delayed output of the shift register (CTL 16 output) is used to set a flip-flop (FFA) to the ONE stage, thereby initiating the pre-inhibit interval necessary to prevent interference with the next sequential ground pulse in the ground pulse train. This following ground pulse terminates the pre-inhibit interval by resetting FFA to the ZERO state. The pre-inhibit interval can vary from 110 to 330 μsecs. The average pre-inhibit interval, however, is on the order of 220 μsecs, which means that approximately four speech pulses are inhibited during each pre-inhibit interval. If for some reason the ground pulse train should end, the pre-inhibit interval is automatically terminated 330 μsecs after its initiation (by CTL 17's output). This description is based upon a system capable of preventing interference with ground pulses coming from one or more tracking radar sets, each operating at a 142 pps rate or at some even multiple of that rate. Some modification would be required in the sync subsystem, primarily in the dividers and register, if a different ground pulse rate were used.

5.3.1.8.4.5 Flip-Flop A

Flip-flop A (FFA) is a bistable multivibrator used to provide pre-inhibit intervals to protect ground pulses from interference. It is set to a ONE state by the delayed output of the 31-stage shift register. It is reset to the ZERO state by the ground pulse next following the ground pulse which initiated operation of the shift register, or by CTL 17's output, as described in 5.3.1.8.4.4, above.

5.3.1.8.4.6 Flip-Flop B

Flip-flop B (FFB) is a bistable multivibrator used in conjunction with a monostable multivibrator (Mono B) to tag certain ground pulses to avoid noise interference, as described in paragraph 5.3.1.5. FFB is set to a ONE state by the output of a core/transistor logic element (CTL 4) in 128D. It is reset to a ZERO state by the output of another core/transistor logic element (CTL 1) in 128D.

5.3.1.8.4.7 Monostable Multivibrator B

Monostable multivibrator B (Mono B) is triggered when FFB is set to the ONE state by any ground pulse which occurs during the 14 μsec modulation interval. The trailing edge of Mono B's 85 μsec pulse is used (in TE) to generate a tag pulse which is transmitted through the beacon and radar receiving antenna to the ground-based decoder.

5.3.1.8.4.8 Divide-by-Eight Divider

Four core/transistor logic elements (CTL's 1, 2, and 3 in 128D, and CTL 14) constitute a divide-by-8 divider (8D). They are used to divide the basic clock frequency of 145,408 pps by 8 to produce audio sampling pulses at a rate of 18,176 pps. These pulses, which have a period of approximately 55 μsecs, are transmitted to the encoder speech processing subsystem.

5.3.1.8.4.9 Monostable Multivibrator A

Monostable multivibrator A (Mono A) is a one-shot monostable multivibrator which is triggered by every pulse which enters the beacon. It is used to provide the post-inhibit interval for the ground pulses. Mono A's output pulse, which has a period of approximately 100 μsecs, inhibits speech and sync pulses only. It does not inhibit ground pulses or tag pulses.

5.3.1.8.4.10 Clock and Ground Pulse Amplifiers

Two core/transistor logic amplifier elements (CTI's 1 and 2) are used to amplify the clock pulses and received ground pulses, respectively.

5.3.1.9 Probability of Ground Pulse Lockout

The probability of lockout of the first N pulses in a ground pulse train is very low. The term lockout, as used here, means blocking of a ground pulse through failure to provide the proper pre-inhibit interval necessary to prevent speech pulses from interfering with one or more ground pulses. The lockout period is approximately 100 μsecs.

The probability of ground pulse lockout was evaluated for various given average speech pulse rates, that is, repetition rates of sampled peaks and troughs in the speech waveform. The results of the evaluation are summarized on Table 5-1. In making the evaluation, it was assumed that any transmitted speech pulse preceding arrival of a ground pulse at the beacon by less than 75 μsecs would cause lockout. Such a situation could occur when the initial pulse in a ground pulse train first arrives at the beacon because there is no way for the encoder system to know in advance when the first pulse in the ground pulse train will arrive.

For a speech rate of 6 kilocycles per second (kc/s), the period is approximately 167 μsecs. The probability of lockout of the first ground pulse is, therefore:

$$\frac{75 \text{ μsecs}}{167 \text{ μsecs}} = 45\%$$

TABLE 5-1

Probability of Ground Pulse Lockout

Ground Pulse Number	Speech Pulse Rate			
	6 kc/s	2 kc/s	1 kc/s	500 cps
1	45%	15%	7.5%	3.8%
2	20%	2.3%	0.56%	0.14%
3	9%	0.34%	0.042%	0.005%
4	4%	0.05%	---	---

and the probability of lockout of two successive ground pulses is:

$$(.45)^2 = 20\%$$

If the average speech pulse rate is assumed to be in the range from 1 to 2 kc/s, inclusive, it can be seen from Table 5-1 that the probability of lockout of N successive ground pulses, where N is equal to 1, 2, 3, or 4, is:

N	1	2	3	4
Lockout Probability (%)	7.5 to 15	0.56 to 2.3	0.042 to 0.34	0.05

5.3.1.10 Encoder/Decoder Waveforms and Timing Functions

A diagram illustrating pertinent waveforms as they appear in the encoder and decoder systems and basic timing relationships between various encoder and decoder system functions is shown on Figure 5-42. It should be noted that:

1. The encoder system accepts a waveform analog of voice data and pulse position modulates it for transmission.

2. The decoder system accepts pulse position modulated data, demodulates it, and produces a synchronous rectangular audio waveform.

The synchronous rectangular audio waveform produced by the decoder system is the delayed inverse of the analog audio waveform accepted by the encoder system. The inversion and delay, however, have no adverse effects upon the intelligibility of the demodulated voice data.

5.3.2 Encoder Speech Processing Subsystem

The encoder speech processing subsystem (ESPS) operates in conjunction with the encoder sync subsystem in preparing voice data for transmission from a spacecraft to a tracking radar via a radar beacon.

The subsystem is designed to:

1. Be compatible with the encoder sync subsystem (ESS).

2. Avoid any interference with the tracking functions of the radar equipment.

3. Provide pulse position modulated (PPM) voice data such that minimum intelligibility is lost in the modulation, transmission, and demodulation processes.

The encoder speech processing subsystem was developed, constructed, in breadboard model form, and tested. Results of the tests conducted on the encoder

speech processing system alone and when operating it in conjunction with the encoder sync subsystem and the decoder system show that the design requirements were successfully met and that the design can be implemented in an operational encoder speech processing subsystem.

5.3.2.1 Encoder Speech Processing Subsystem Logic and Components

5.3.2.1.1 General

The encoder speech processing subsystem is designed to convert a speech waveform into a pulse train for transmission to a tracking radar via a radar beacon. The pulses in the train are pulse position modulated (PPM) with respect to basic clock pulses in such a manner that an intelligible facsimile of the speech waveform can be reconstructed by a suitable decoder.

A logic diagram of the encoder speech processing subsystem is shown on Figure 5-43.

5.3.2.1.2 Subsystem Functional Requirements

Analysis of design requirements for an encoder speech processing subsystem capable of processing speech in a manner suitable for transmission via a radar beacon indicated that the subsystem must perform the following-listed functions:

1. Derive from the speech waveform the amplitude and frequency information required to describe the waveform with sufficient accuracy as to minimize loss of voice data intelligibility.

2. Encode the amplitude and frequency information derived from the speech waveform by employment of a pulse position modulation technique in which the pulses representing frequency and amplitude information are modulated in time with respect to a basic clock pulse train.

3. Transmit the pulse position modulated signal to the radar beacon.

5.3.2.1.3 Component Functional Requirements

The following list identifies and indicates the principal functional requirements of the essential components required to mechanize the encoder speech processing subsystem logic.

1. Audio input source. This is generally a magnetic tape recorder.

2. An audio amplifier (AMP) used to provide sufficient gain to assure that the regenerative clipper will be able to operate over a broad dynamic range.

3. A filter (FL) which limits the audio signal bandwidth by attenuating frequencies above 3,000 cycles per second (cps). The circuit is shown schematically on Figure 5-44.

4. Several differentiators (D1, D2, and D3) which apply a uniform 6 decibels (db) per octave slope for low frequencies. The differentiators each consist essentially of a single resistance-capacitance (RC) section. The differentiator circuit is shown in schematic diagram form on Figure 4-45.

5. An integrator (INT) which applies a 6db per octave slope for high frequencies. The circuit used is shown schematically on Figure 5-46.

6. A regenerative clipper (CLP) used to provide a square wave output signal in response to a speech analog waveform. This is done to enable better definition of the waveform's zero crossings. The circuit is shown schematically on Figure 5-47.

7. A phase inverter (PI) which inverts the output signal of the regenerative clipper. The phase inverter is similar to that described in paragraph 5.3.1.7.6.11 and shown schematically on Figure 5-39.

8. A flip-flop (FF1) which is used to perform essential logic functions. It can be set or reset. This flip-flop is similar to that described in paragraph 5.3.1.7.6.4 and shown schematically on Figure 5-32.

9. A leading edge pulse generator (LEPG). This is a differentiating-type circuit employed to provide an output pulse coincident with the leading edge of a square wave pulse. The circuit is shown in schematic diagram form on Figure 5-48.

10. Three trailing edge pulse generators (TEPG1, TEPG2, and TEPG3). Each is used to produce a pulse coincident with the trailing edge of a square wave pulse. Although the circuit is similar to that used in the leading edge pulse generator, it differs in that it contains an inverter element. The circuit is shown schematically on Figure 5-49.

11. Two monostable multivibrators (MS1 and MS2). Each is used to generate an output voltage for a finite period of time following receipt of an appropriate input, or triggering, signal. At the end of that time the output voltage returns to the quiescent state level. These multivibrators are similar to those described in paragraph 5.3.1.7.6.7 and shown schematically on Figure 5-35.

12. A sampler (SAM). The sampler continuosly monitors the amplitude of an applied waveform and, when triggered, places a specific charge on a capacitor in a pulse modulation monostable multivibrator. The amount of charge is proportionate to the voltage level of the waveform at the time the sampler is triggered. A schematic diagram of the sampler circuit is shown on Figure 5-50.

13. A pulse modulation monostable multivibrator (PMS) which is used to provide delayed pulses. The circuit is that of a modified monostable multivibrator. When it is triggered, it provides a delayed output pulse. The delay is proportionate to the amount of charge on a capacitor in the multivibrator circuit. This is the capacitor charged by the sampler. A schematic diagram of the pulse modulation monostable multivibrator circuit is shown on Figure 5-51.

14. Three OR gates (OR1, OR2, and OR3) are used. In each case, an output signal is produced in response to any one of several input signals or to any combination of such signals. The circuit is similar to that described in paragraph 5.3.1.7.6.9 and shown schematically on Figure 5-37.

15. An AND gate (A) is used to perform essential logic functions. It provides an output signal only when all of its input signals are present simultaneously. The circuit is similar to that described in paragraph 5.3.1.7.6.8 and shown schematically on Figure 5-36.

16. Two inhibit AND gates (AI1 and AI2) are used. In each case the gate allows a signal received at its signal input terminal to be transmitted from the signal output terminal except when another signal (the inhibiting signal) is simultaneously present at the gate's inhibit input terminal. The circuit used is similar to that described in paragraph 5.3.1.7.6.10 and shown schematically on Figure 5-38.

5.3.2.1.4 Logic Operation

Operation of the encoder speech processing subsystem is described in paragraphs 5.3.2.1.4.1 and 5.3.2.1.4.2 and their subparagraphs.

5.3.2.1.4.1 Peak/Trough Pulse Generation

The peak/trough (P/T) pulse generation portion of the encoder speech processing subsystem logic provides pulse-type signals coincident with the peaks and troughs of an audio input signal. These pulse-type signals are referred to in this report as peak/trough (P/T) pulses. They are produced as follows.

An audio input signal is amplified and then differentiated in (DI), filtered by FL, and then processed by the regenerative clipper (CLP). The output of the regenerative clipper is sent to both a phase inverter (PI) and a second differentiator (D2). The output signal from the phase inverter is again differentiated, in D3. The output signals from differentiators D2 and D3 are applied to the input terminals of an OR gate (O1) whose output provides pulses coincident with the peaks or troughs of the amplified audio input signal. The output of the filter (FL) is also used to drive a low output

impedance type of integrator (INT) whose output signal within the 3 kilocycles per second (kc/s) pass band of the low-pass filter approximates the true amplified audio signal. The peaks and troughs of the integrator's output coincide with the P/T pulses provided by the OR gate (O1).

5.3.2.1.4.2 Clock Pulse Selection and Sampling

The clock pulse selection and sampling logic selects the clock pulses to be encoded with audio signal amplitude information and performs the encoding. Generally, the first clock pulse to occur following a peak or trough in the amplified audio input signal is selected for encoding and subsequent transmission as a pulse position modulated (PPM) pulse, as described in paragraph 5.3.2.1.4.2.1. Occasionally there are deviations from this technique, as explained in paragraph 5.3.2.1.4.2.2. For a further discussion of the sampling process, see paragraph 5.3.2.2.

5.3.2.1.4.2.1 Signal-Correlated Sampling

In the signal-correlated sampling and encoding approach the peak/trough (P/T) pulses operate to set a flip-flop to a ONE state (FFI). Concurrently, gated clock pulses are applied to FFI at a constant rate to reset it to a ZERO state. The first P/T pulse to occur sets FFI whose output is applied to an AND gate (A1), a leading edge pulse generator (LEPG), and a trailing edge pulse generator (TEPG1). The output signal from the leading edge pulse generator produces a pulse which turns on a monostable multivibrator (MS2) via an inhibit AND gate (AI1) and an OR gate (O2). The output of the multivibrator is used, via an OR gate (O3) and an inhibit AND gate (AI2), to prevent clock pulses from resetting FF1 to a ZERO state during the ON period of the monostable multivibrator (MS2). The period during which the multivibrator (MS2) is ON represents the sampling period during which the sampler (SAM), triggered by the output of the multivibrator (MS2), places a charge on a capacitor in the pulse modulation monostable multivibrator (PMS). The amount of charge corresponds to the amplitude of the audio waveform at the output of the integrator (INT). The first clock pulse to occur, after the sampling period, is then selected to reset FF1 and to generate a pulse, through a trailing edge pulse generator (TEPG1), to trigger the pulse modulation monostable multivibrator (PMS). The period of this multivibrator is directly proportional to the charge placed on its capacitor by the sampler (SAM). At the end of the period during which the pulse modulation monostable multivibrator (PMS) was ON, a pulse is applied through a trailing edge pulse generator (TEPG3) to a beacon trigger circuit. The pulse from trailing edge pulse generator (TEPG1) is also used to trigger a monostable multivibrator (MS1) to provide a post-inhibit interval during which no clock pulses can be selected.

5.3.2.1.4.2.2 Non-Signal-Correlated Sampling

In the signal-correlated sampling approach described in paragraph 5.3.2.1.4.2.1, one or more P/T pulses may occasionally occur during the post-inhibit inter-

val. Sampling cannot be accomplished when this occurs because the sampler (SAM) cannot be triggered since flip-flop 1 (FF1) will be set to a ONE state.

As an alternative to this approach, a non-signal-correlated sampling technique is employed. In this technique, a trailing edge pulse generator (TEPG2) triggers the monostable multivibrator (MS2) whose output is then used to trigger the sampler (SAM). This enables sampling to take place. From that point on, operation of the subsystem is the same as in the signal-correlated sampling technique, with the exception that the sample read into the pulse modulation monostable multivibrator (PMS), in the form of a charge placed by the sampler (SAM) on a capacitor in the multivibrator, and subsequently transmitted to the beacon is a non-signal correlated sample of the amplitude of the audio input waveform.

5.3.2.2 Sampling Process

Use of a high clock pulse rate to increase the "P/T pulse/selected clock pulse" timing accuracy made it necessary to provide a post-inhibit interval. Suitable logic has been incorporated, therefore, in the encoder speech processing subsystem to perform this function.

In the signal-correlated sampling process, the post-inhibit interval inhibits sampling if a P/T pulse closely follows a previously selected clock pulse. This has certain undesirable consequences.

If a third P/T pulse does not arrive for a considerable period of time subsequent to the end of the post-inhibit interval, the level of the sample taken in response to the first P/T pulse is retained in the decoder for an inordinate length of time, since no signal will have been received which could alter the level. As a result, the facsimile waveform produced by the decoder would be distorted and such distortion would adversely affect the quality of the speech reproduction.

Deletion of any audio pulses from transmission causes some degradation of the facsimile waveform. Since a certain number of such pulses would be lost as a result of designing the system to assure protection of the radar tracking pulse train against interference by extraneous pulses, it became imperative to avoid unnecessary deletions. Accordingly, the non-correlated sampling technique was adopted to complement the sample correlated technique. This not only makes it possible to terminate the otherwise erroneously prolonged level as it eventually appears in the decoder's output, but also, by furnishing a sample (although an uncorrelated one) of the speech waveform, supplies the decoder with correct amplitude information after the post-inhibit interval. This information would be lacking if the signal-correlated sampling approach alone were used.

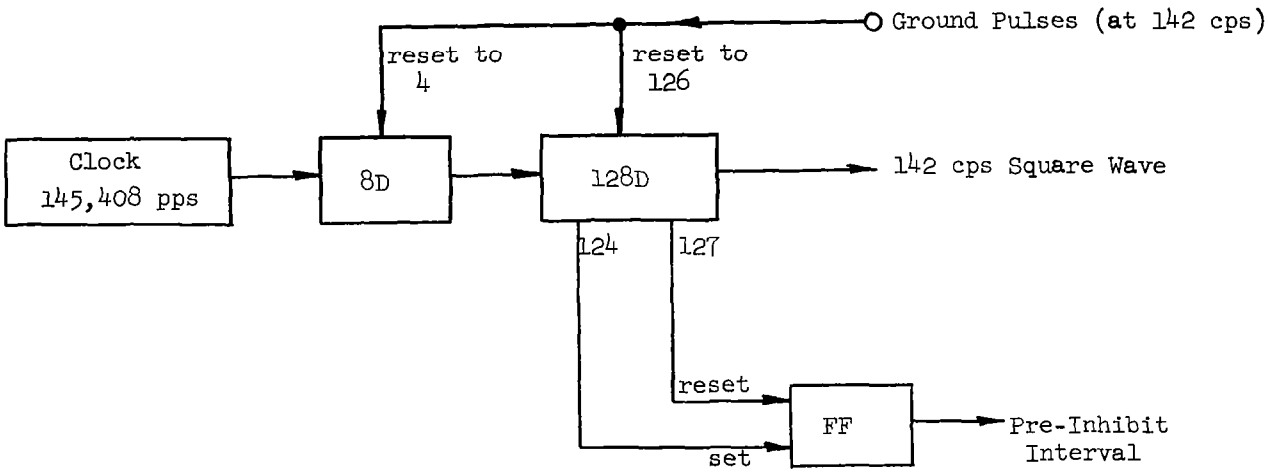


Figure 5-4. Block Diagram, Basic Clock Rate Divider

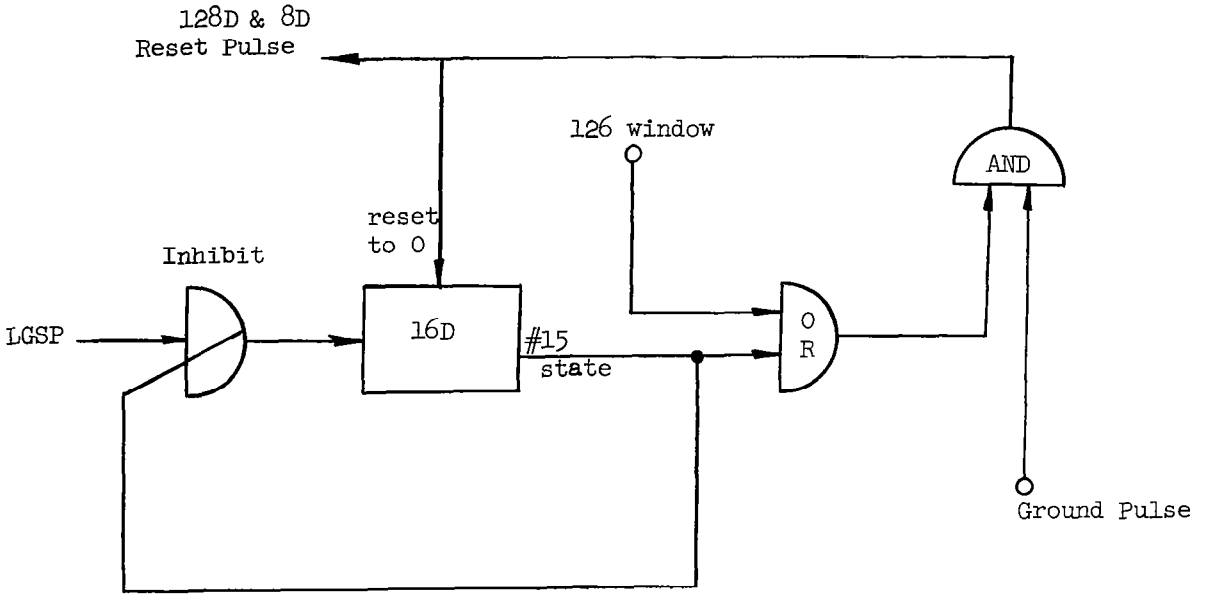


Figure 5-5. Logic Arrangement, Divide-by-Sixteen Divider

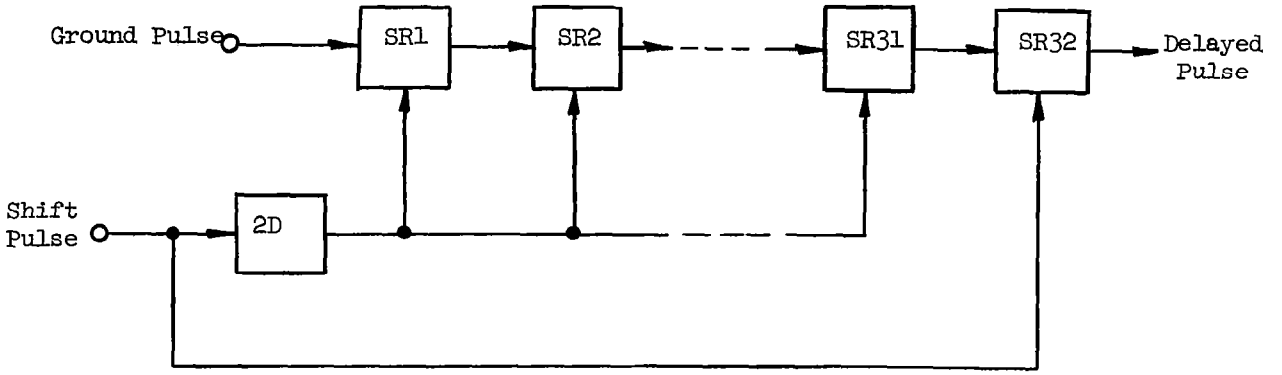


Figure 5-6. Logic Arrangement, Thirty-two Stage Shift Register

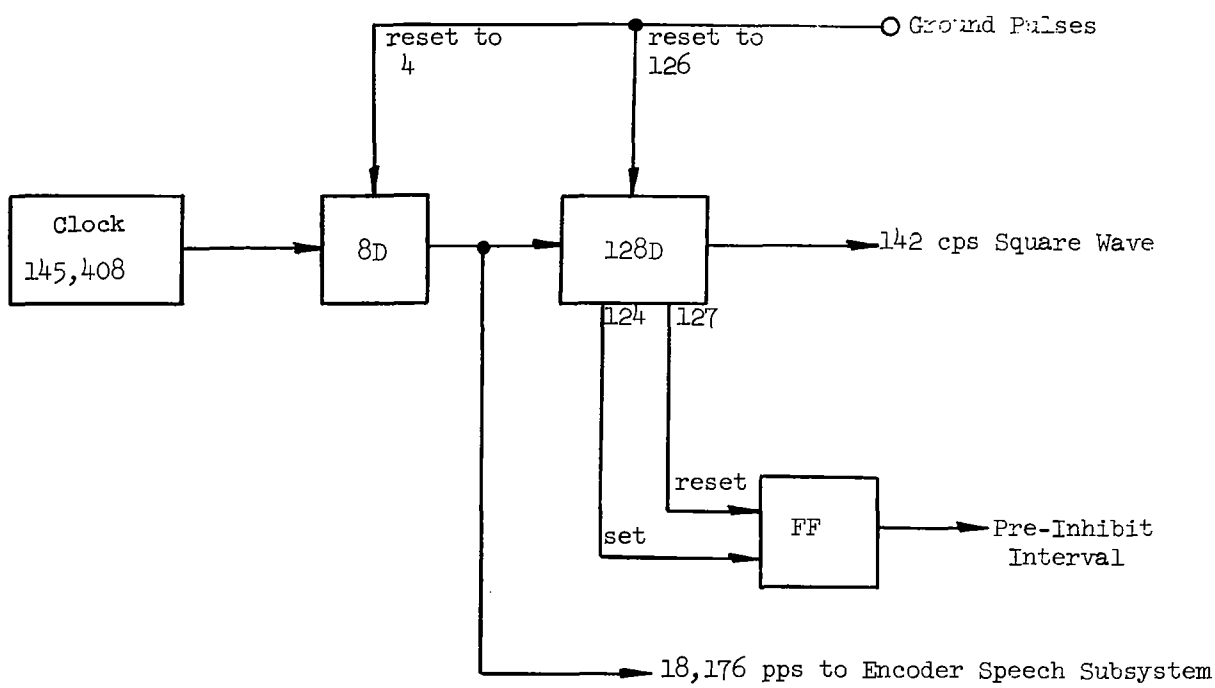


Figure 5-7. Block Diagram, Basic Clock Rate Divider and Sync Pulse Source

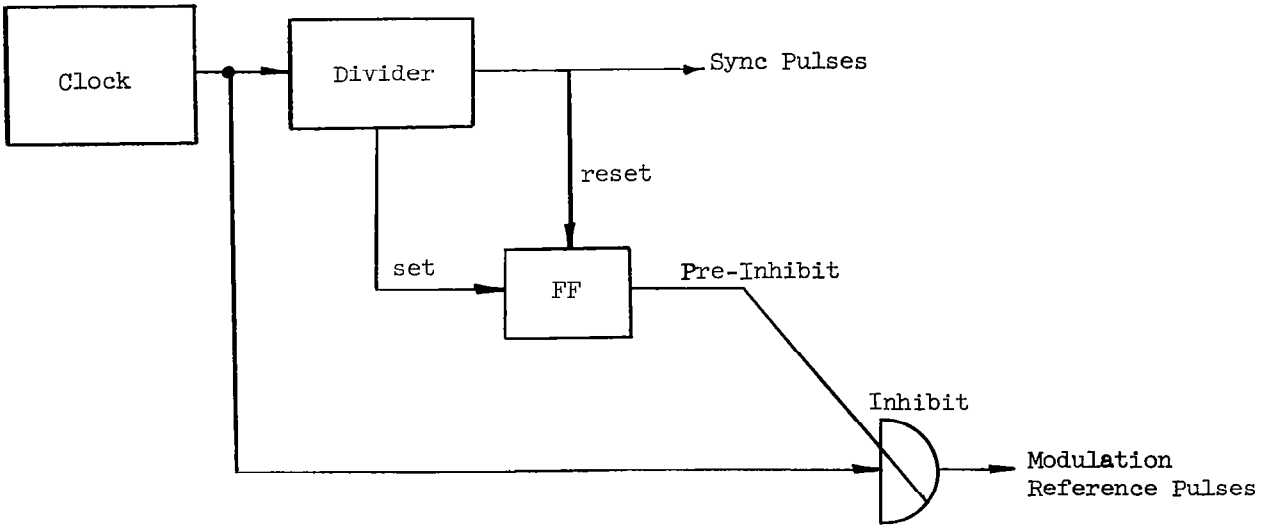


Figure 5-8. Logic Arrangement, Encoder-Generated Sync Pulse Source

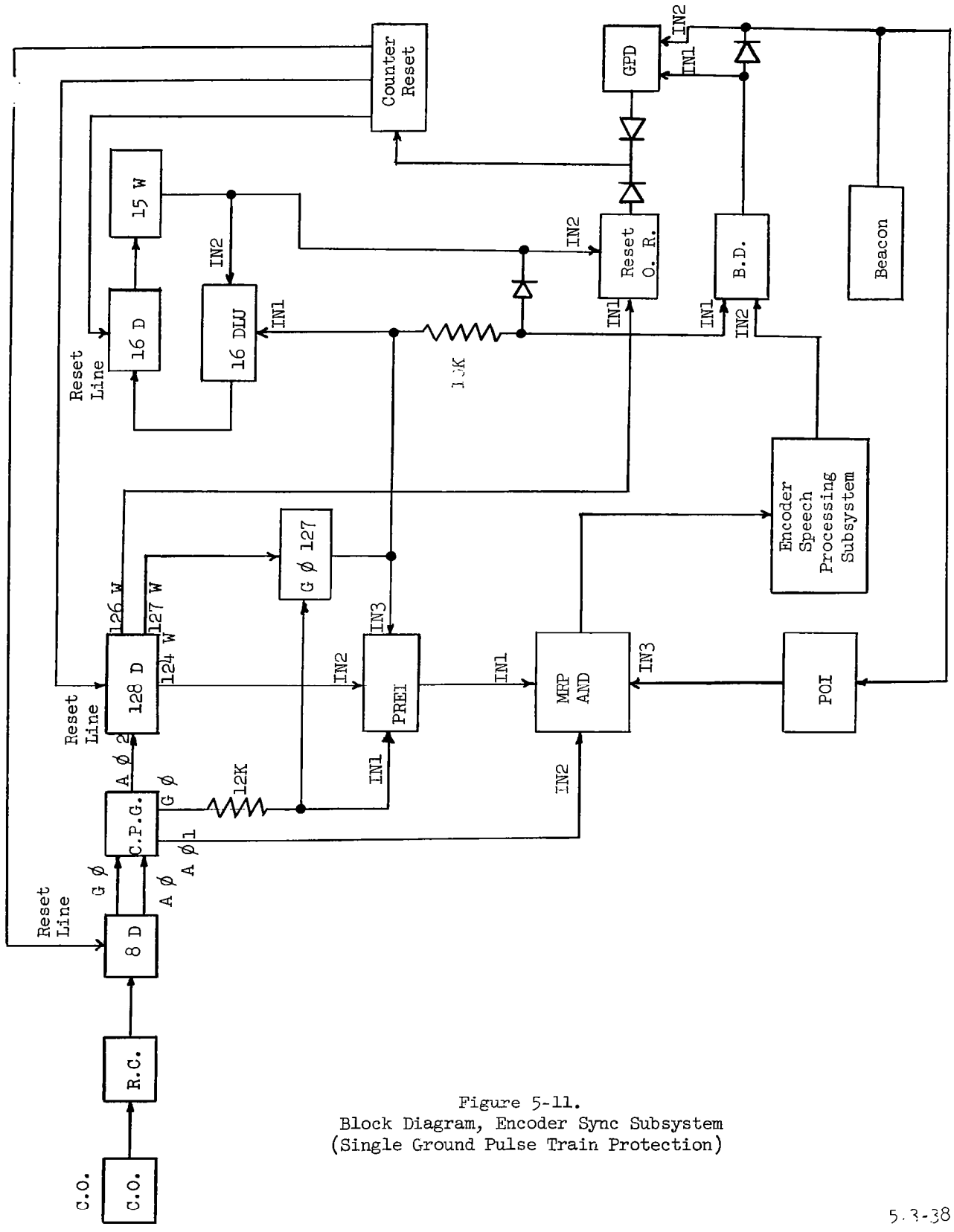
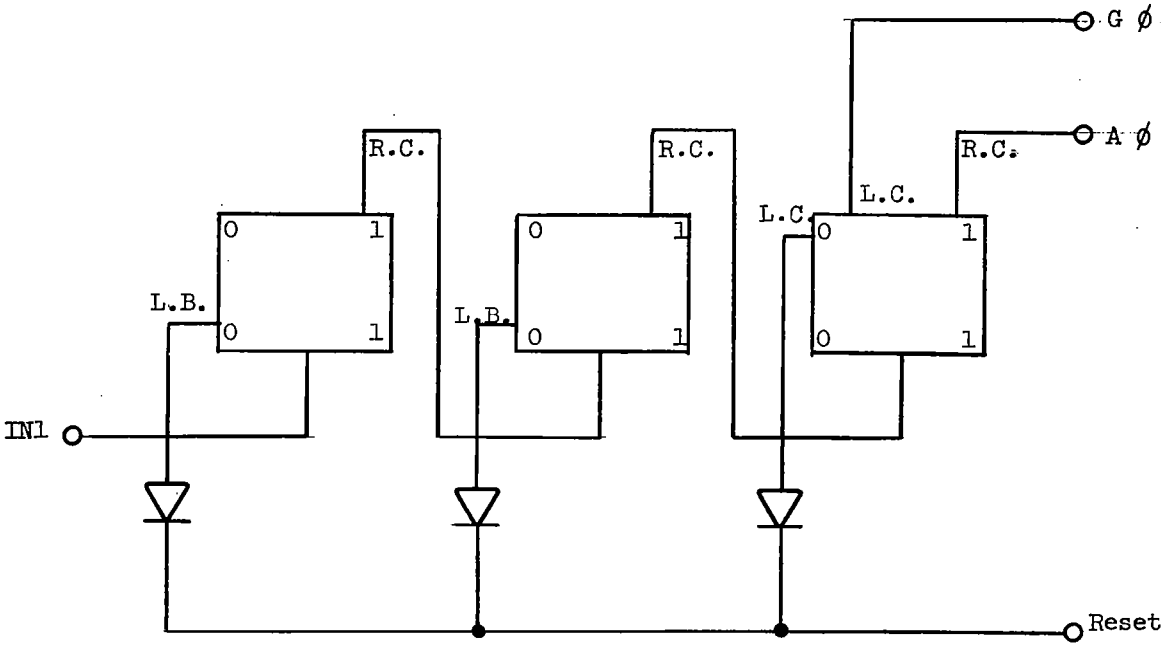


Figure 5-11.
Block Diagram, Encoder Sync Subsystem
(Single Ground Pulse Train Protection)



L.C. Left Collector
R.C. Right Collector
L.B. Left Base
R.B. Right Base

Figure 5-12. Logic Arrangement, Divide-by-Eight Divider

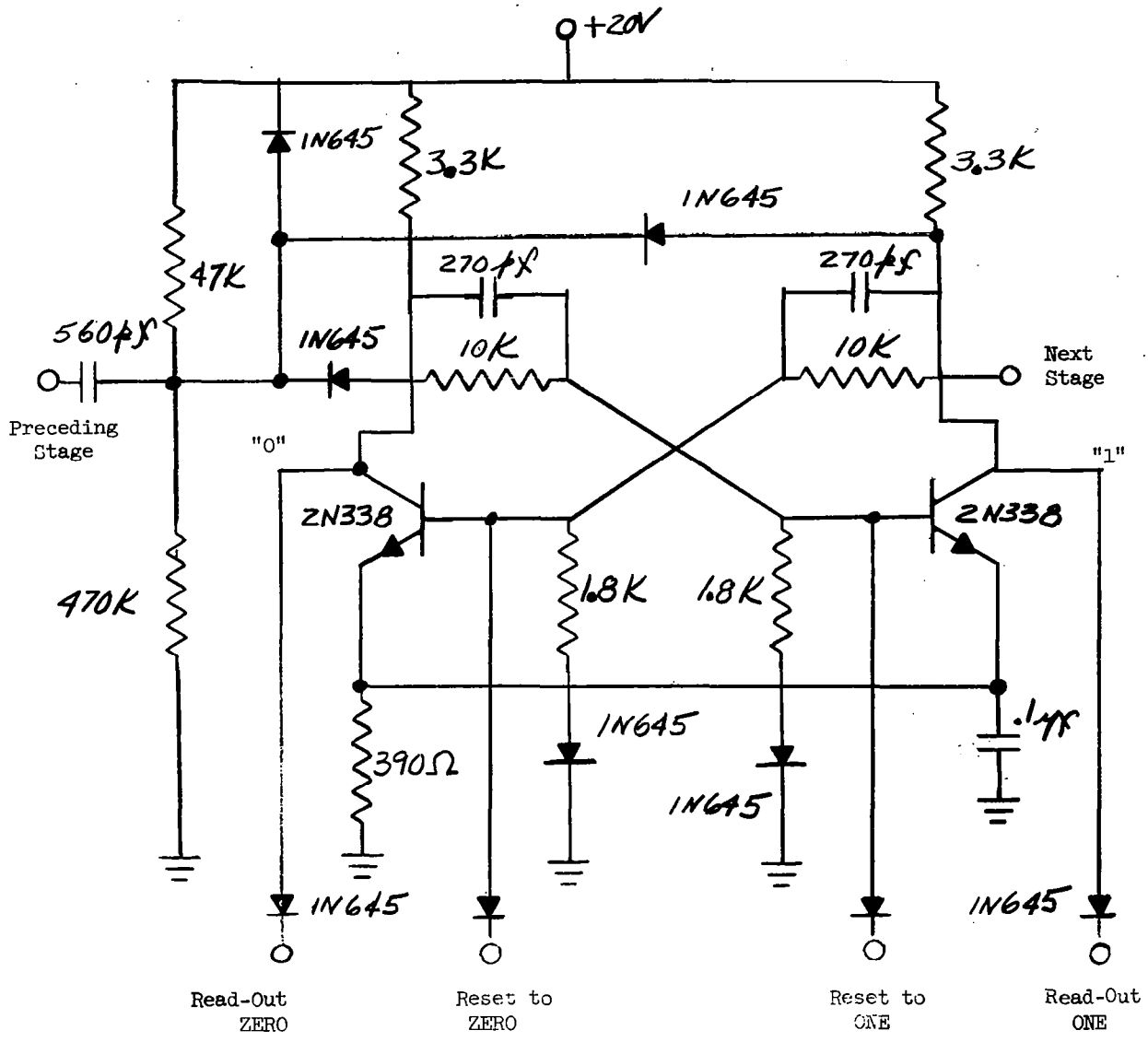


Figure 5-13. Schematic Diagram, One Stage of Divide-by-Eight Divider

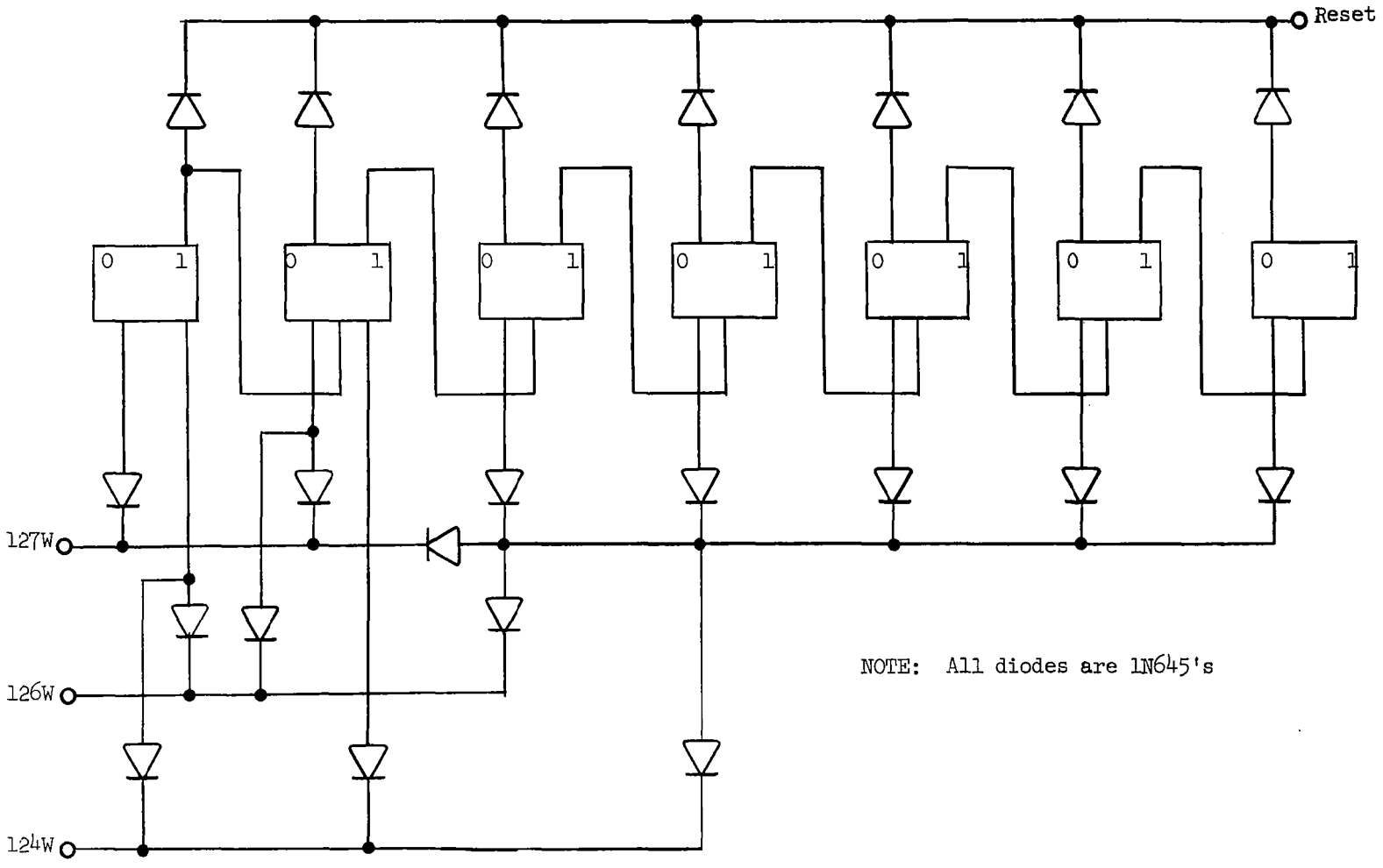


Figure 5-14. Logic Arrangement, Divide-by-128 Divider

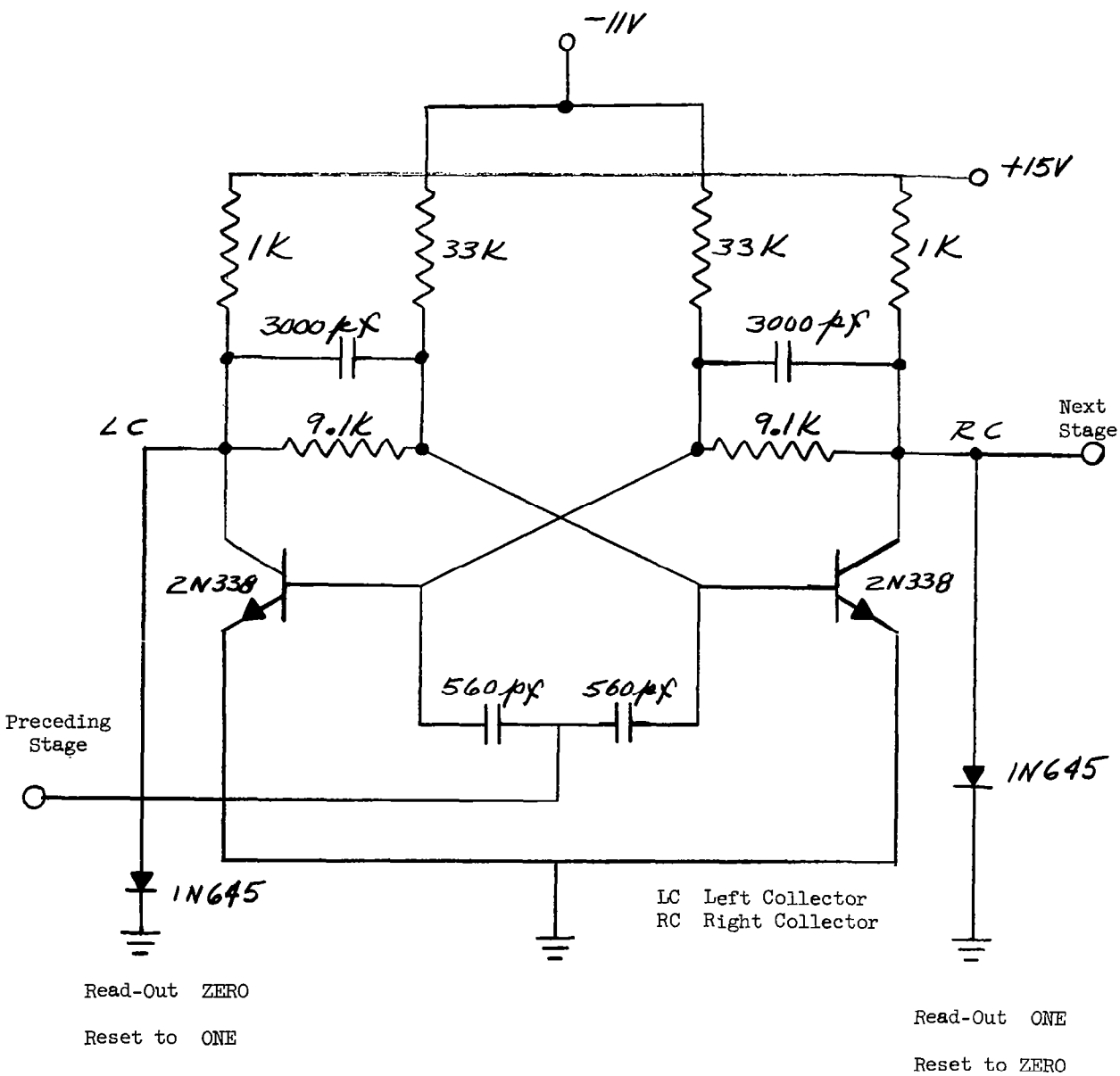


Figure 5-15. Schematic Diagram, One Stage of Divide-by-128 Divider

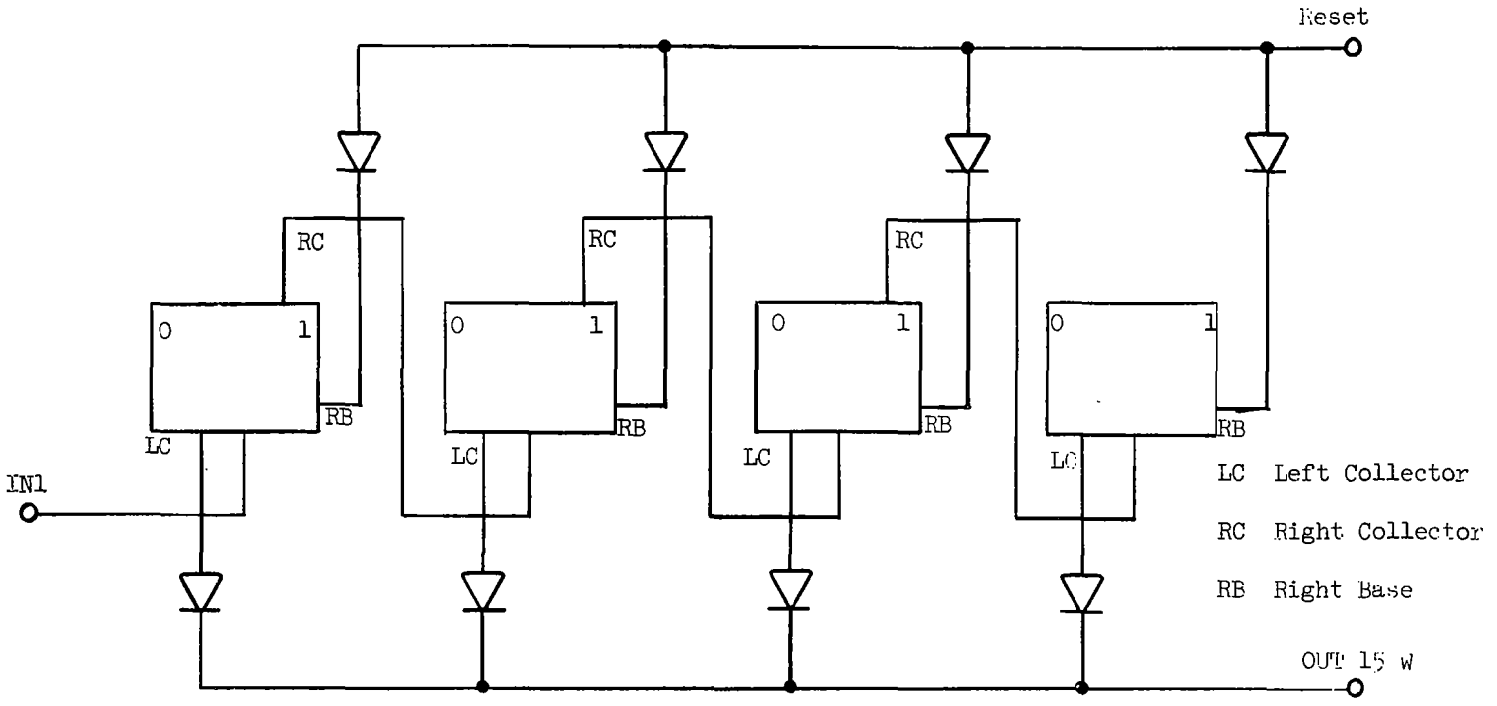


Figure 5-16.
Logic Arrangement, Divide-by-16 Divider

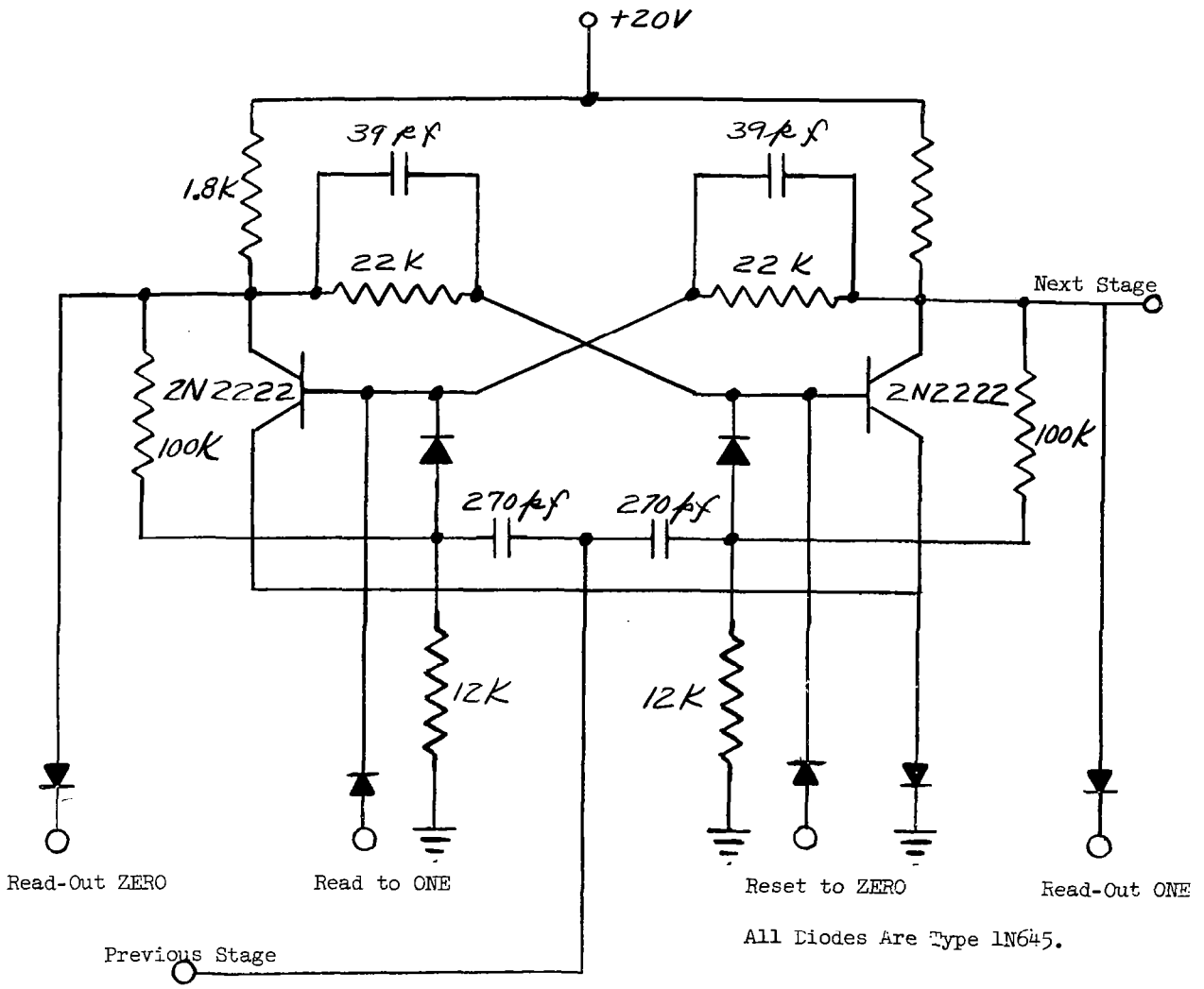


Figure 5-17.
Schematic Diagram, One Stage of Divide-by-16 Divider

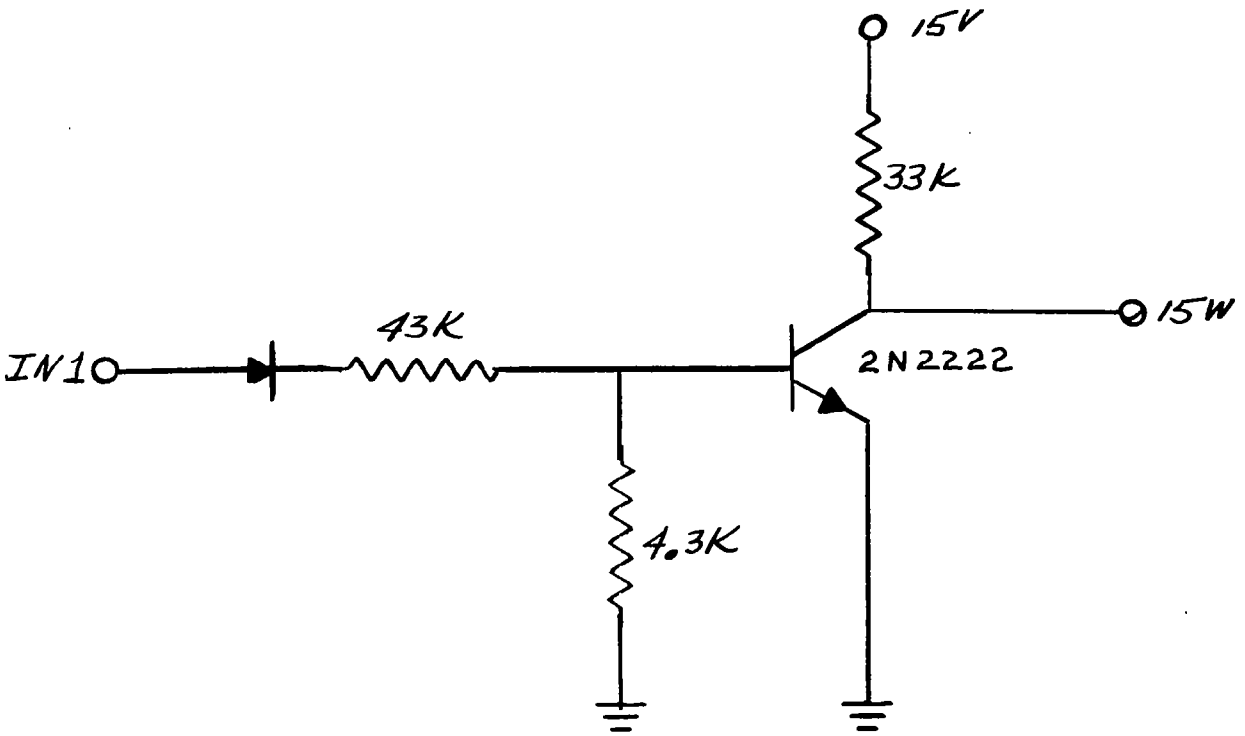


Figure 5-18.
Schematic Diagram, 15-Window

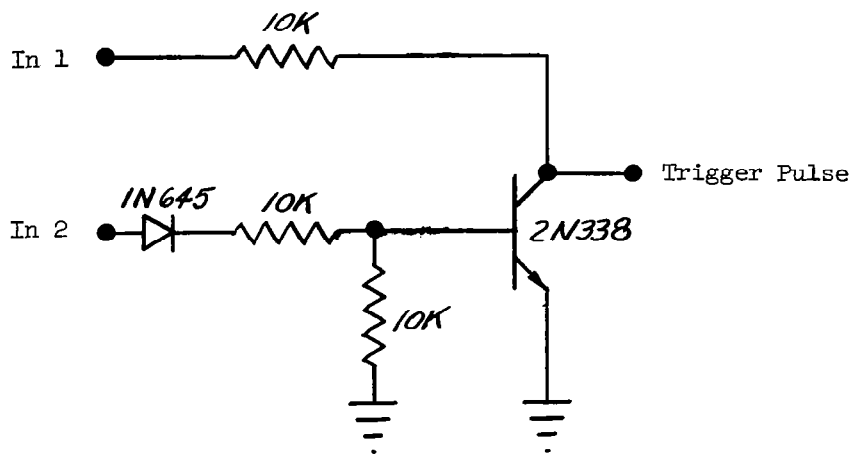


Figure 5-19.
Schematic Diagram, Divide-by-16 Divider Lock-up

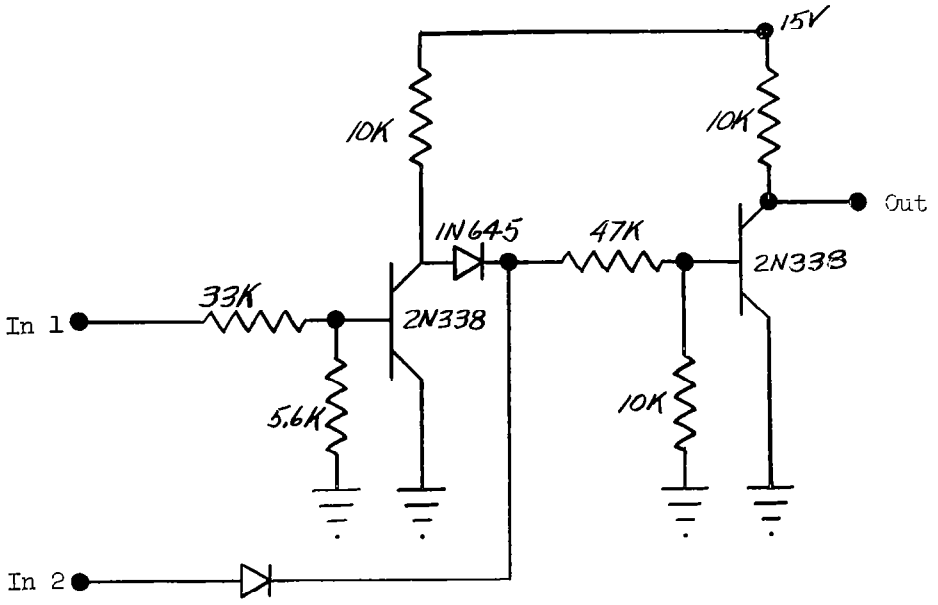


Figure 5-2C.
Schematic Diagram, Reset OR Circuit

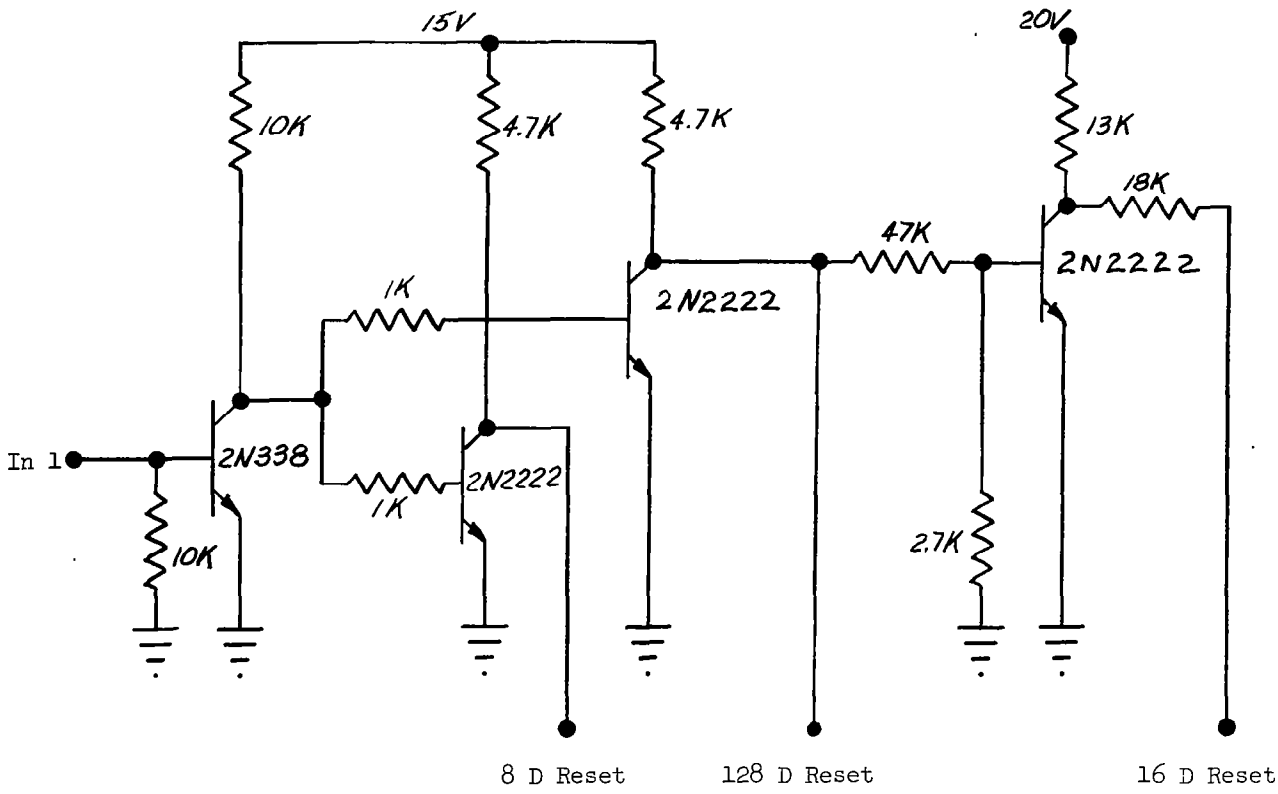


Figure 5-21.
Schematic Diagram, Counter Reset Circuit

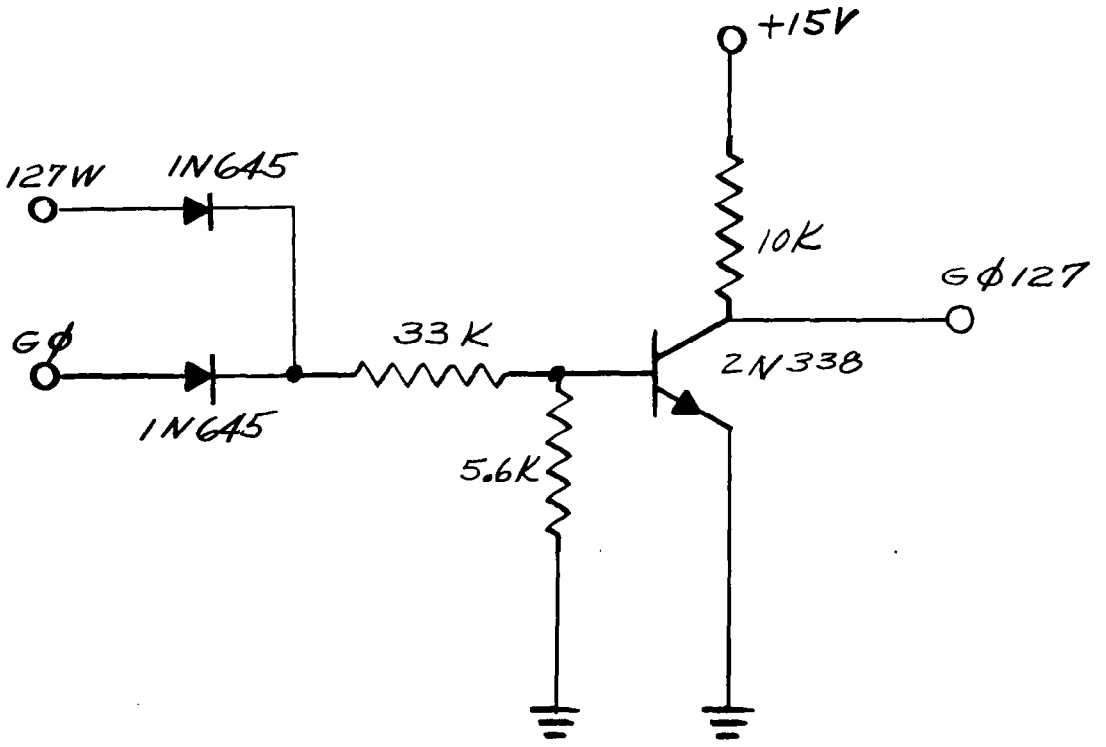


Figure 5-22.
Schematic Diagram, G ϕ 127 AND Gate

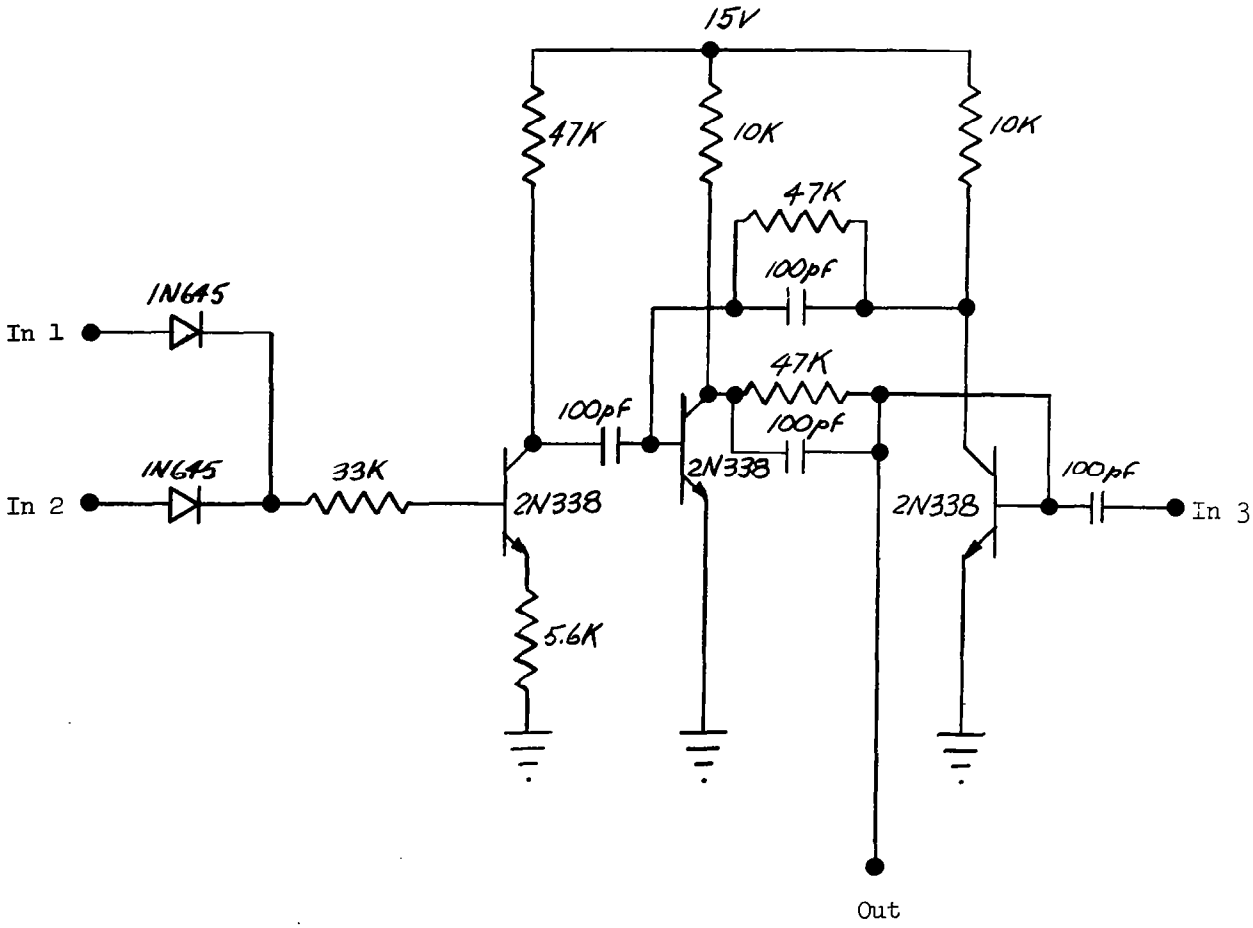


Figure 5-23.
Schematic Diagram, Pre-Inhibit Flip-Flop

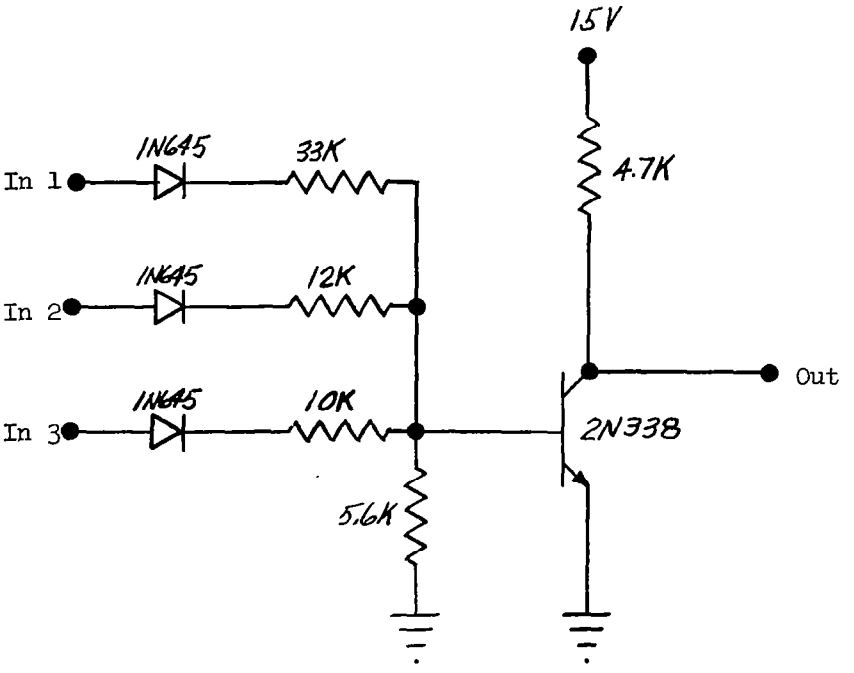


Figure 5-24.
Schematic Diagram, Modulation Reference Pulse AND Gate

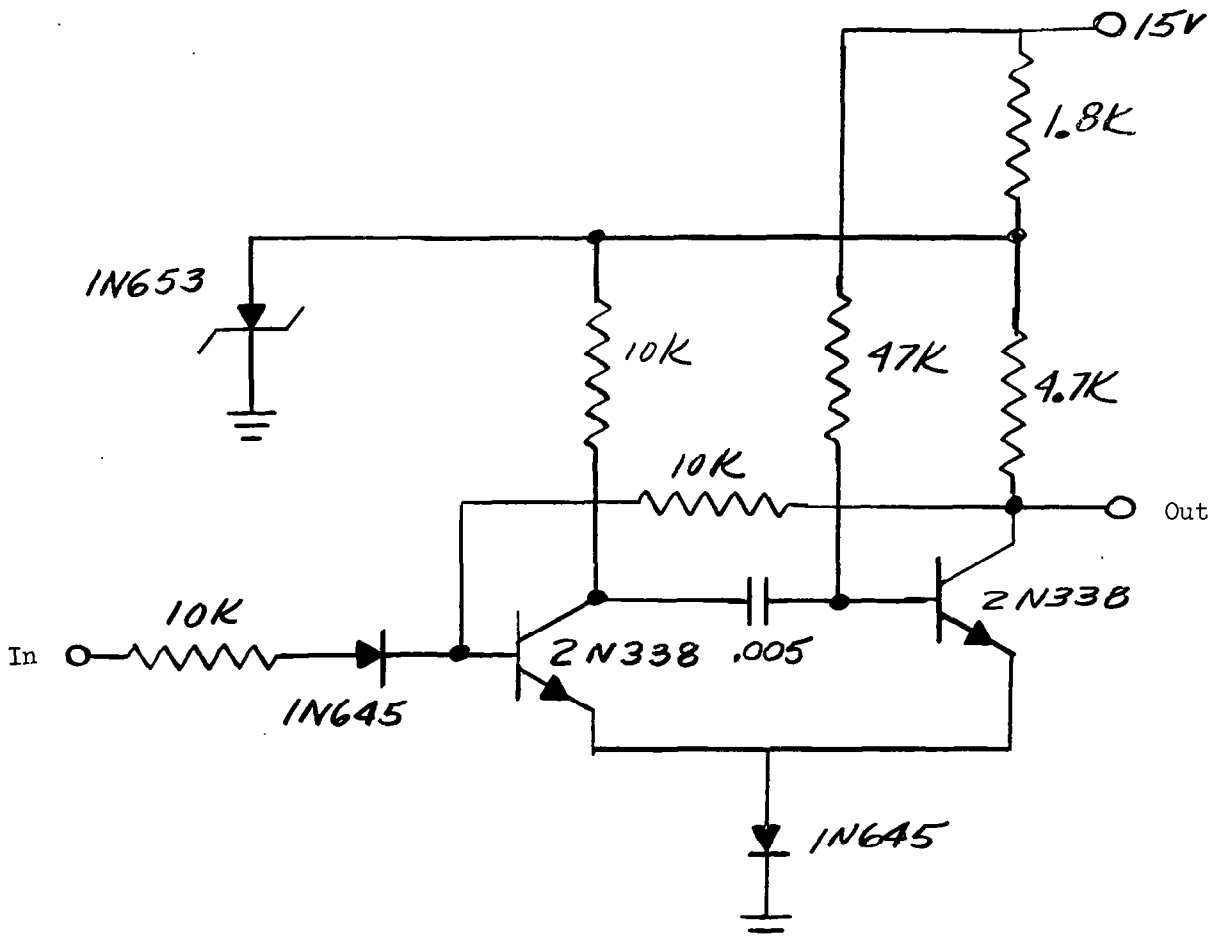


Figure 5-25.
Schematic Diagram, Post-Inhibit Monostable Multivibrator

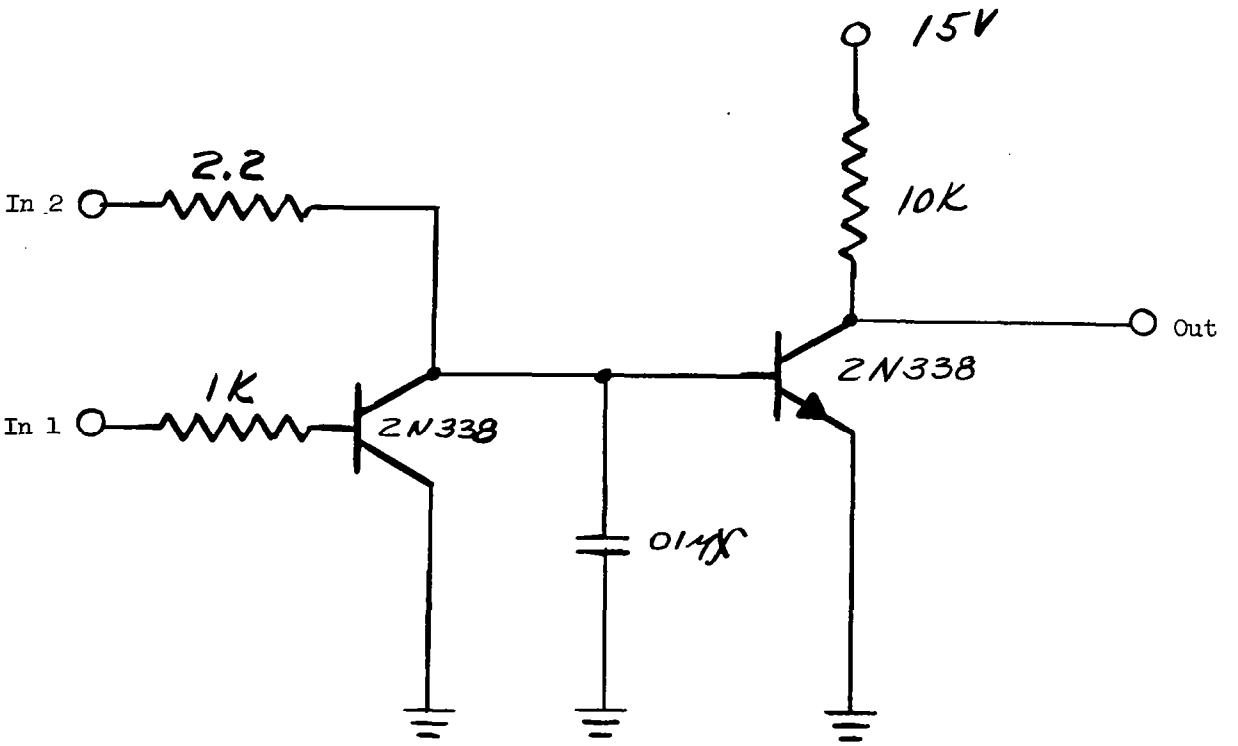


Figure 5-26.
Schematic Diagram, Ground Pulse Detector

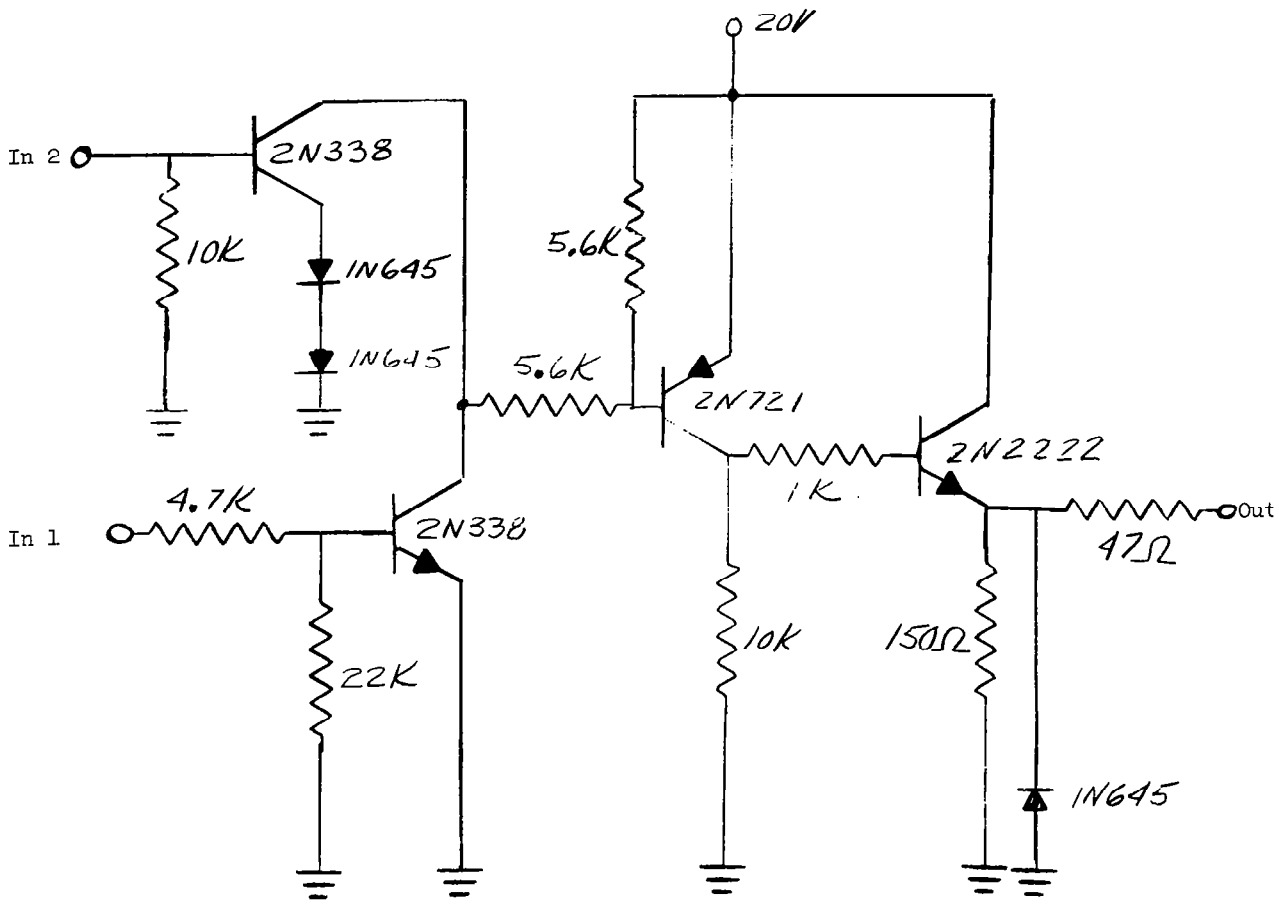


Figure 5-27.
Schematic Diagram, Beacon Driver

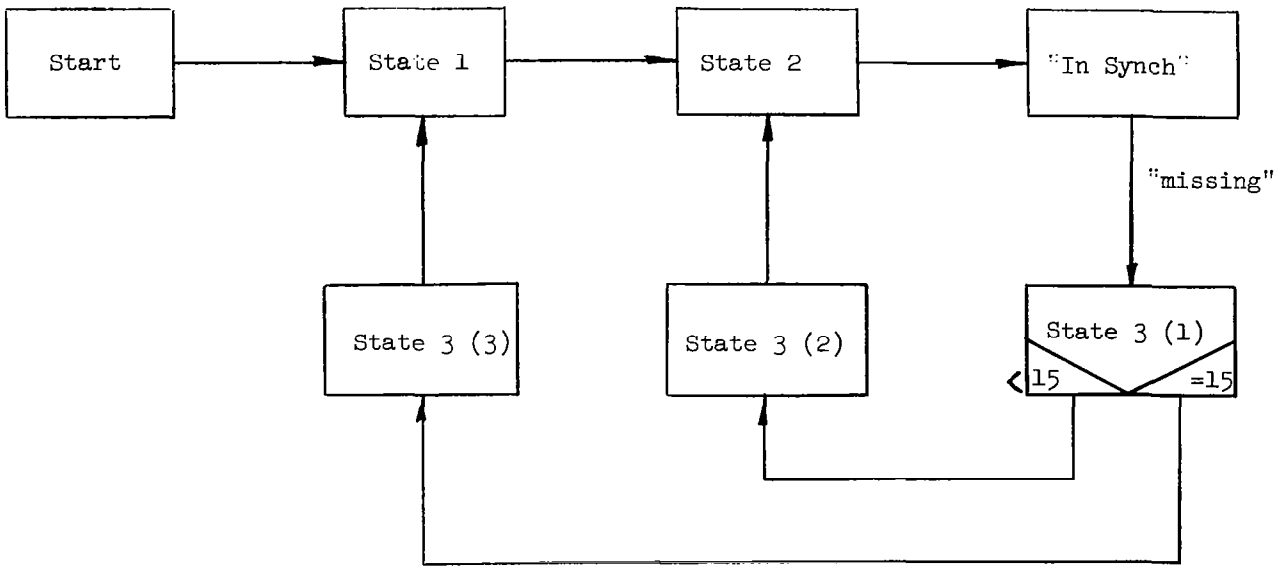


Figure 5-28.
Flow Diagram, Encoder Sync Subsystem Logic States
(Single Ground Pulse Train Protection)

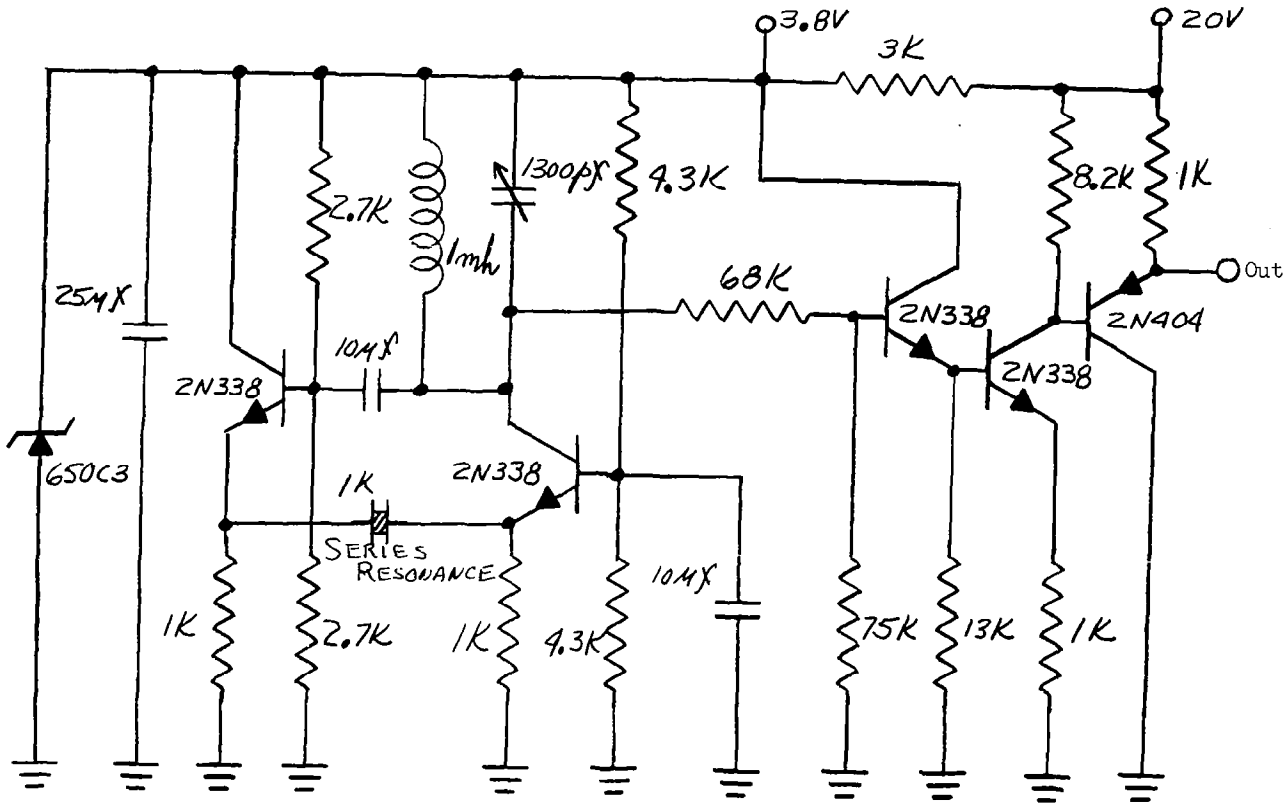


Figure 5-29.
Schematic Diagram, Crystal-Controlled Oscillator

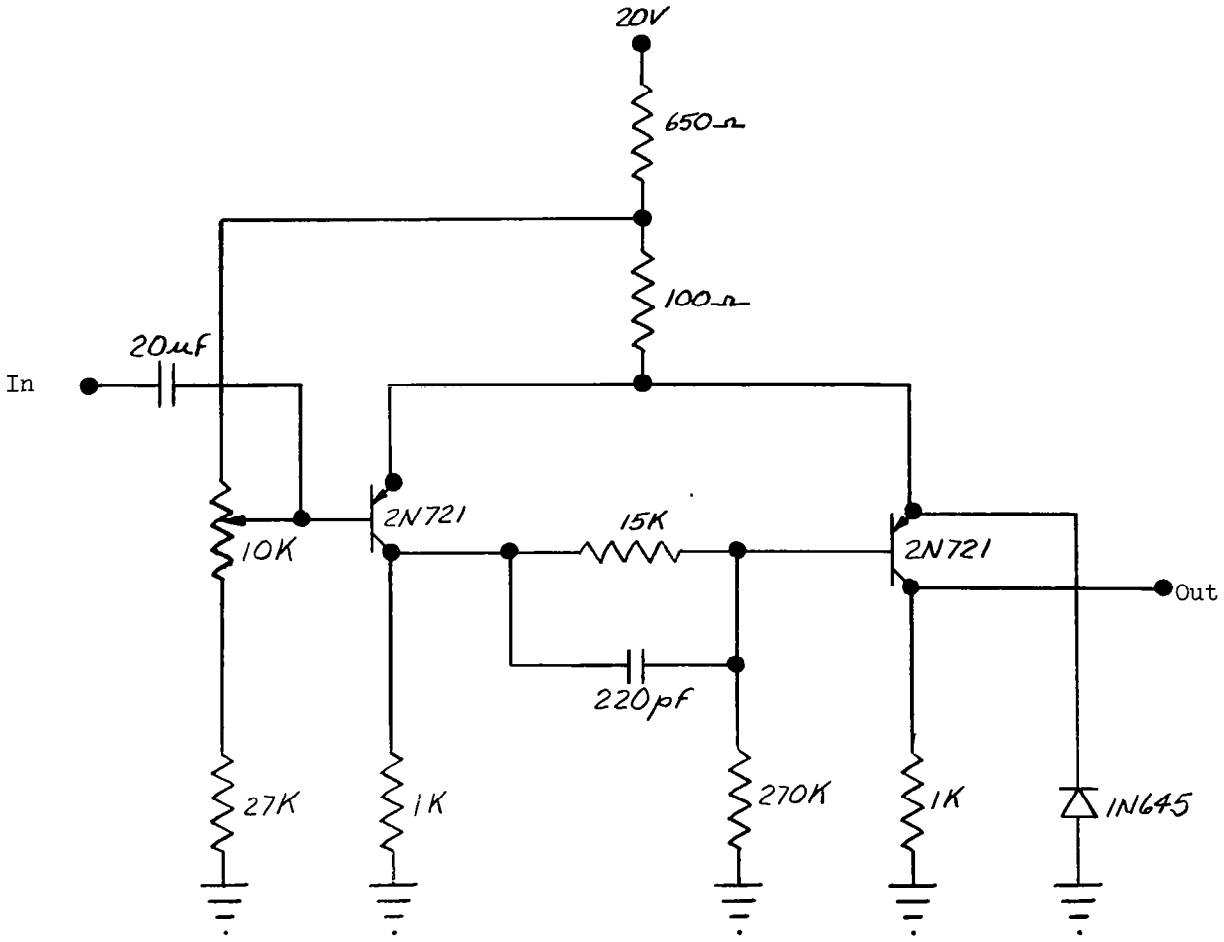


Figure 5-30.
Schematic Diagram, Regenerative Clipper

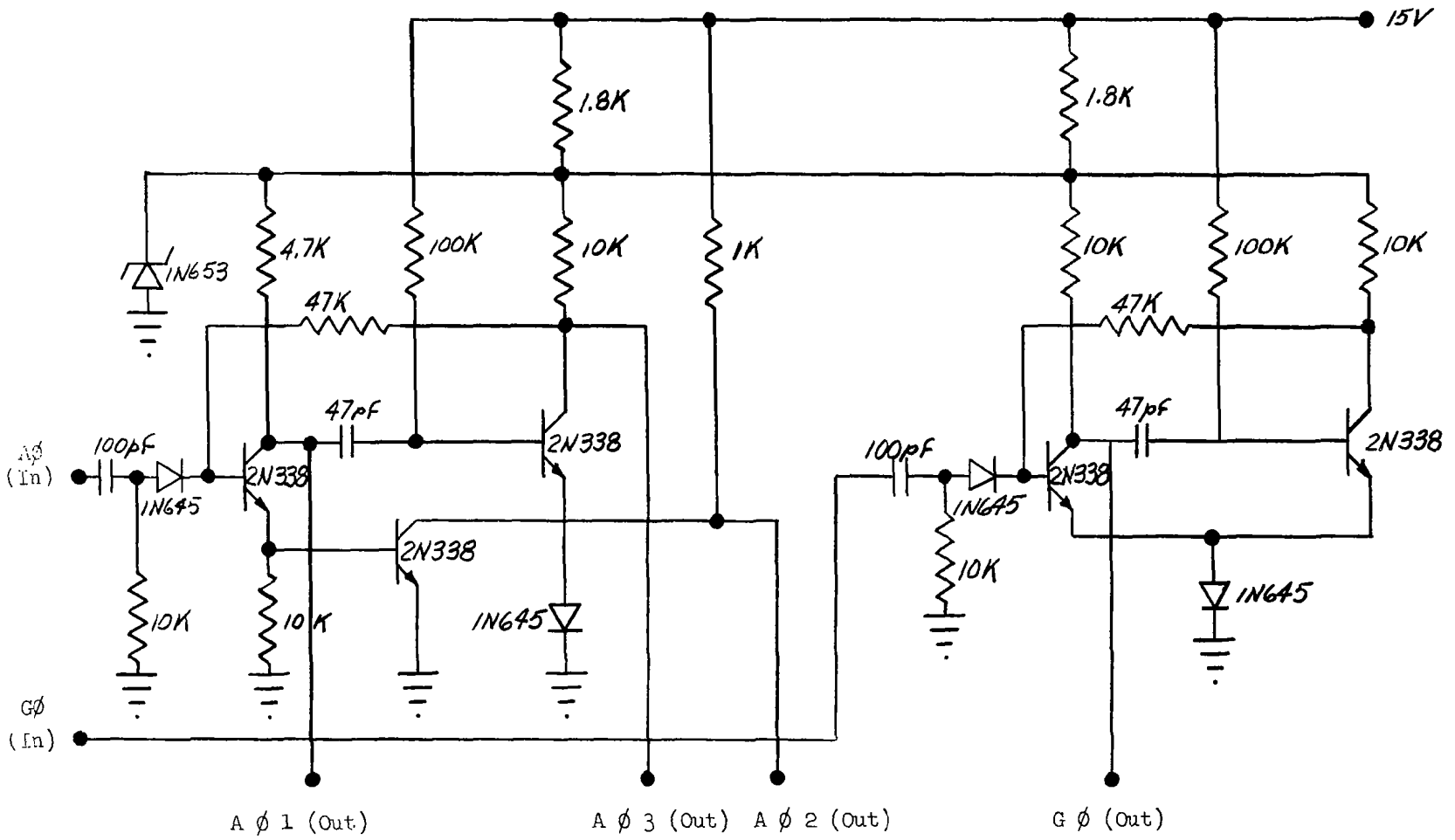


Figure 5-31.
Schematic Diagram, Clock Pulse Generator

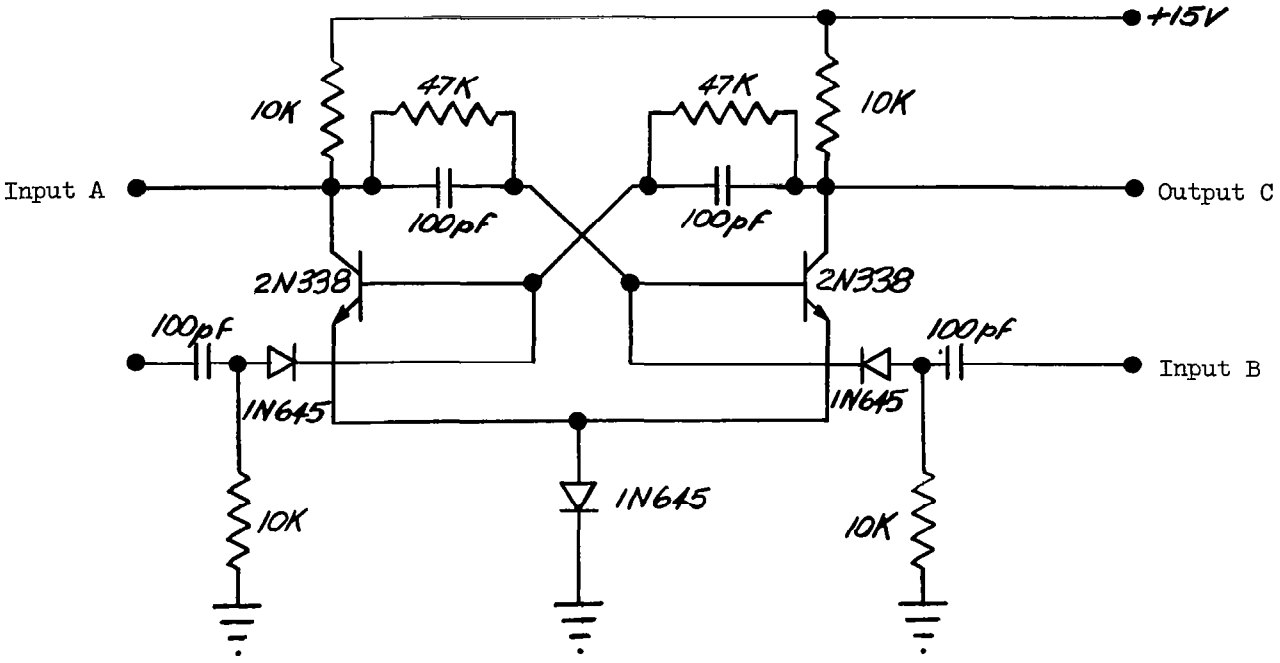


Figure 5-32.
Schematic Diagram, Typical Set-Reset Type Bistable Multivibrator

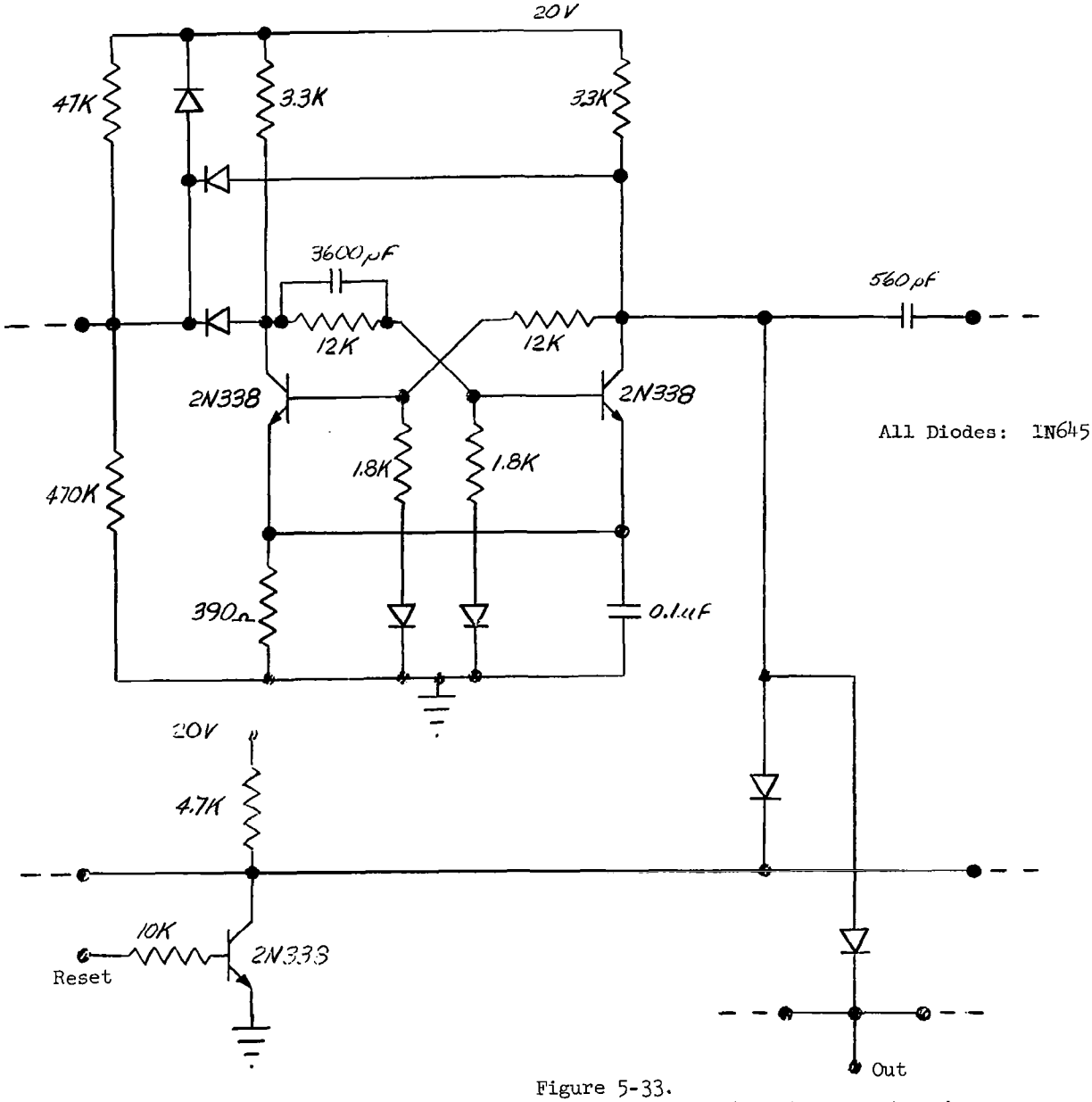


Figure 5-33.
Schematic Diagram, Triggered Bistable Multivibrator, Type A

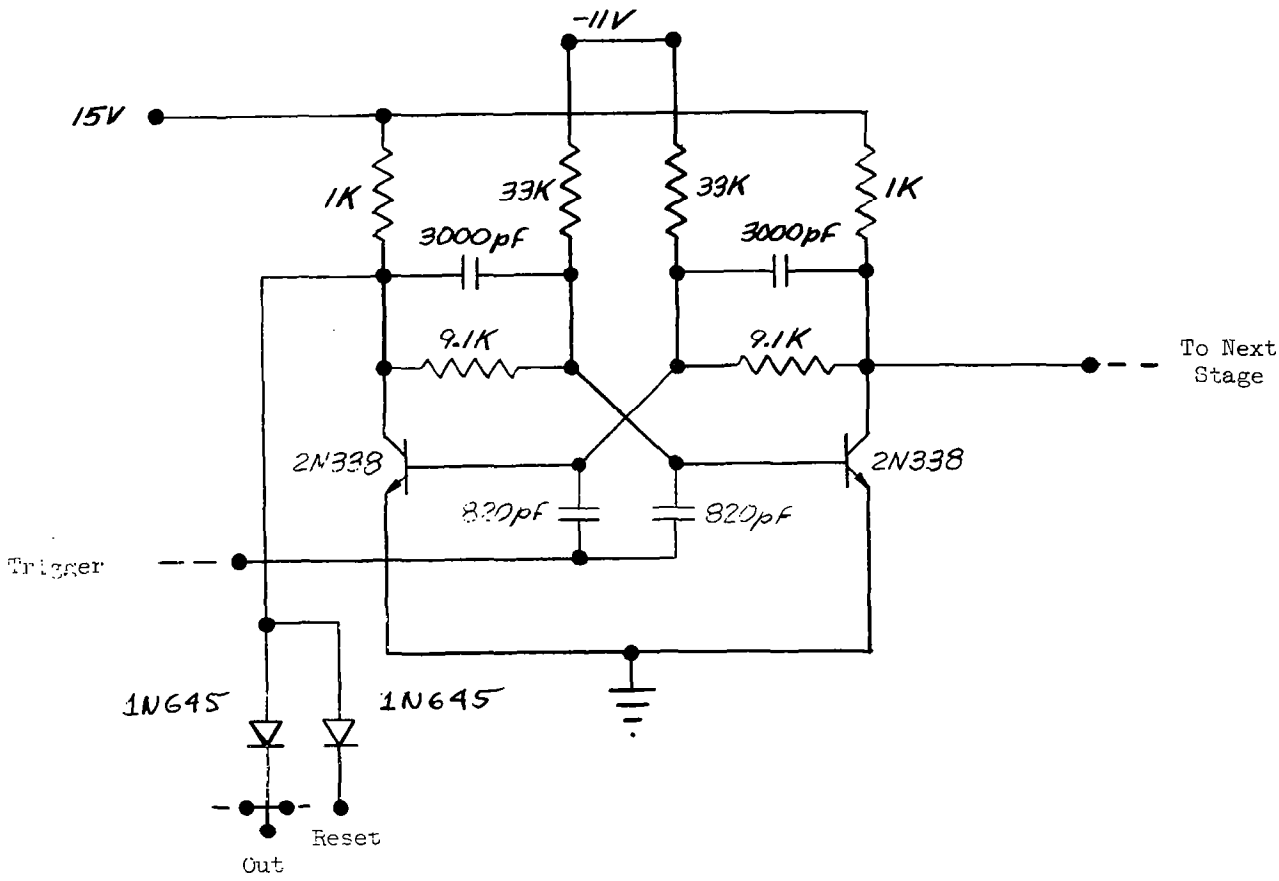


Figure 5-34.
Schematic Diagram, Triggered Bistable Multivibrator, Type B

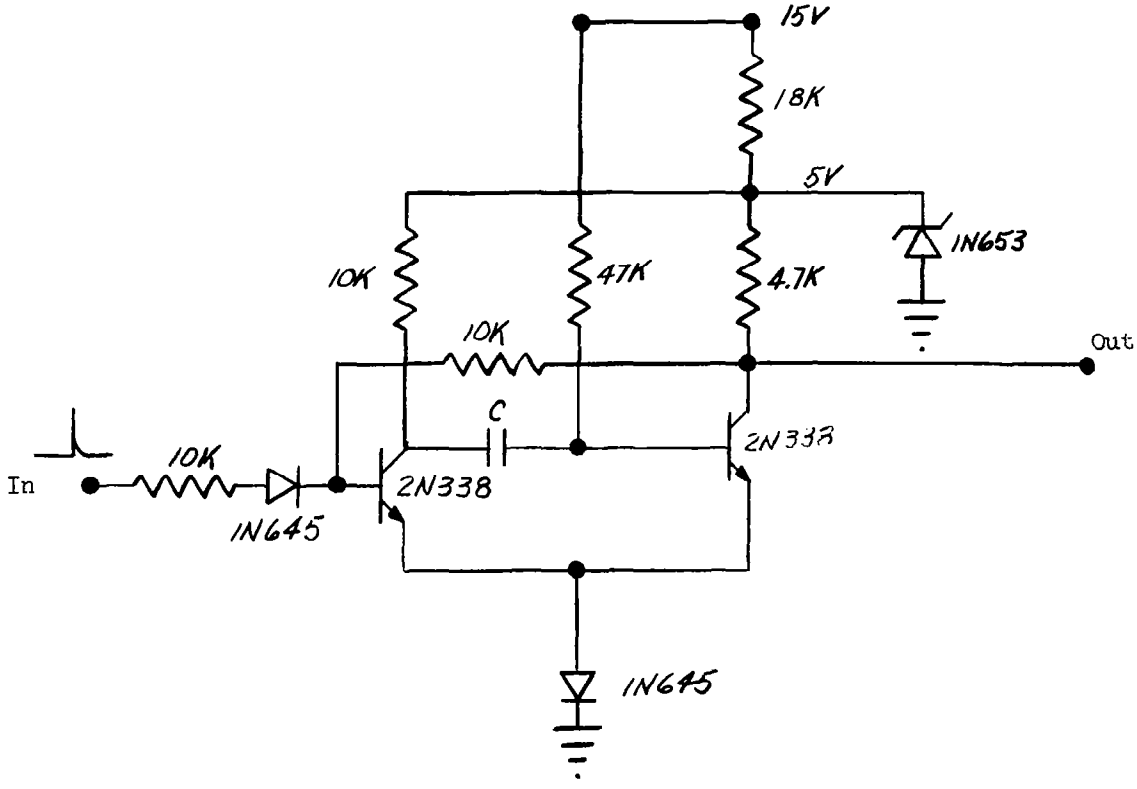


Figure 5-35. Schematic Diagram, Monostable Multivibrator

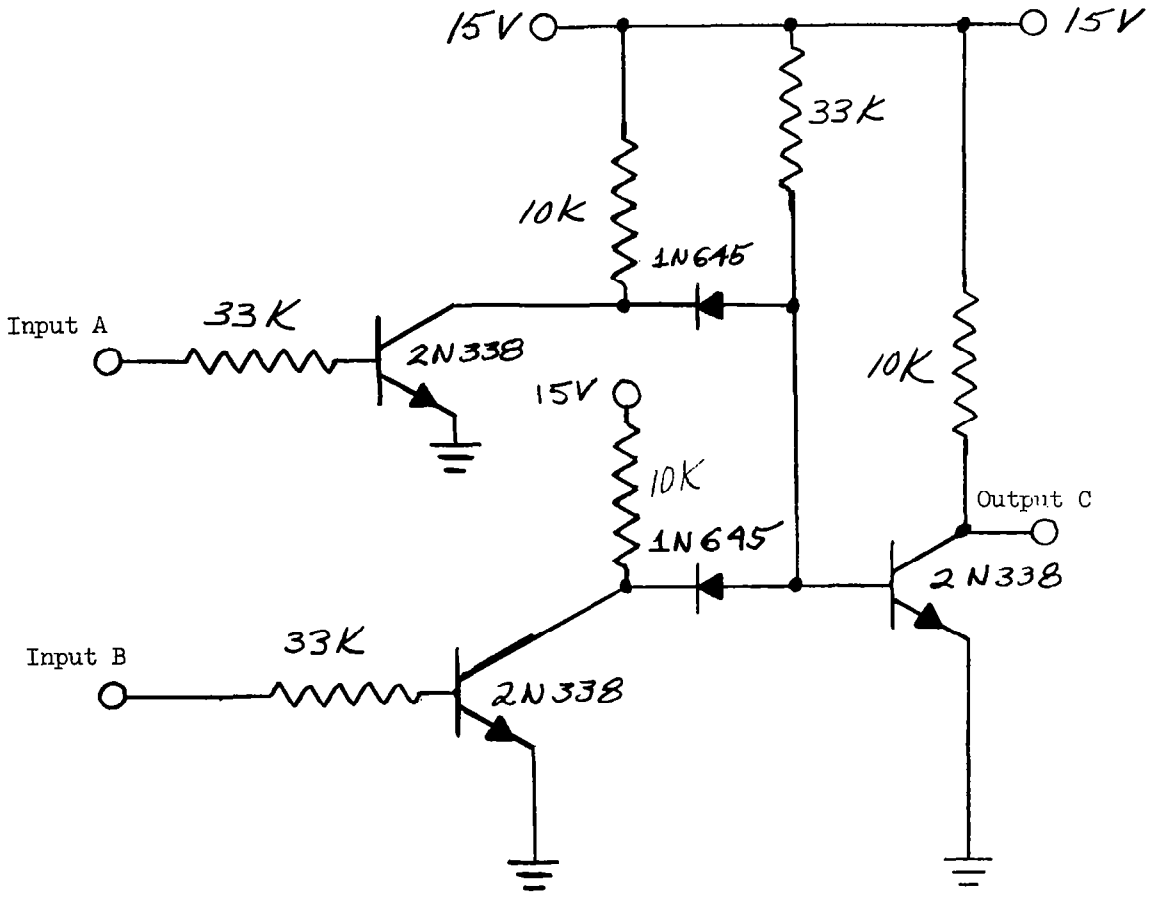


Figure 5-36.
Schematic Diagram, Typical AND Gate

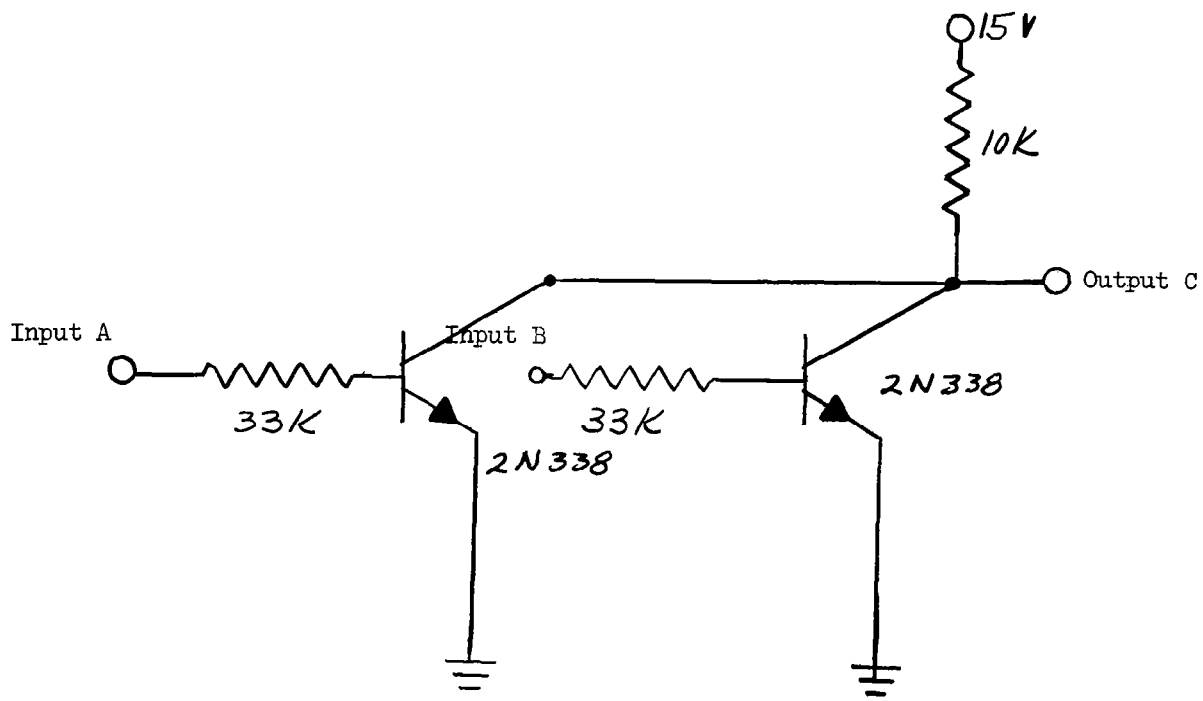


Figure 5-37.
Schematic Diagram, Typical OR Gate

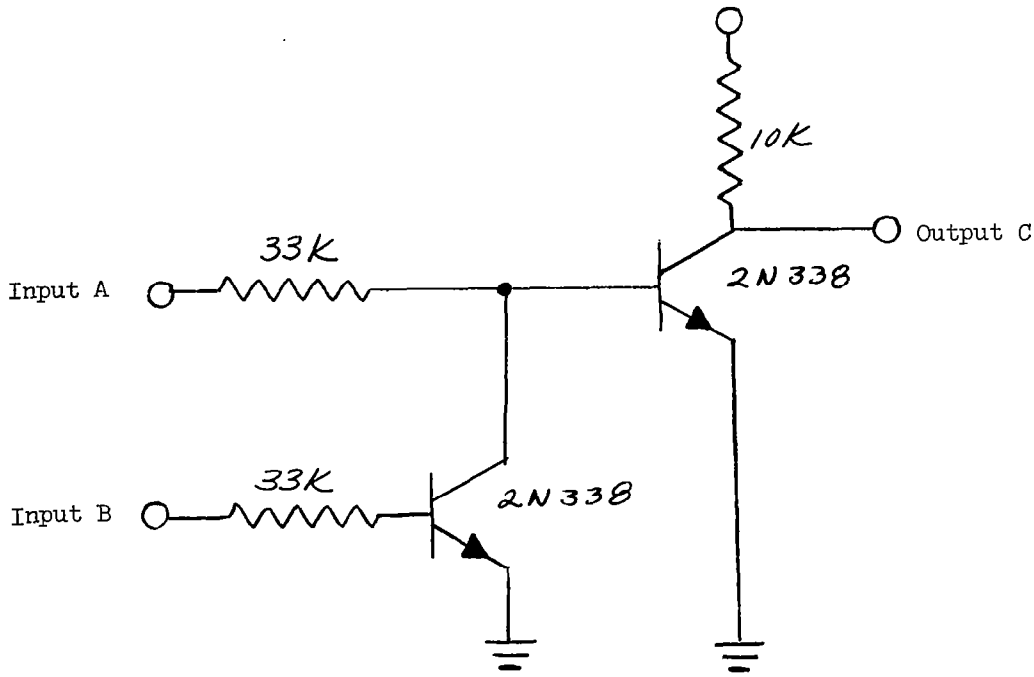


Figure 5-38.
Schematic Diagram, Typical Inhibit Gate

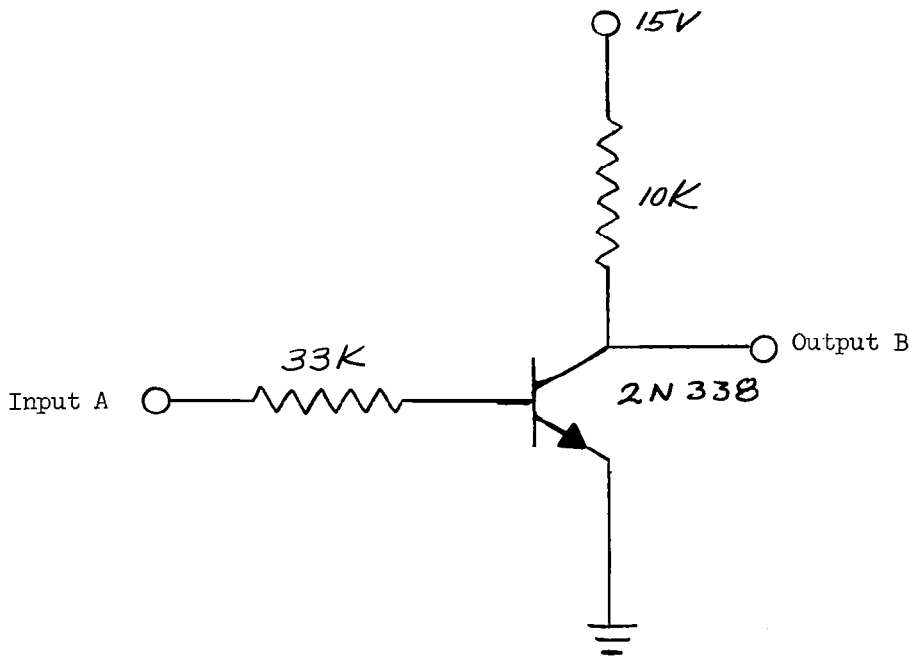


Figure 5-39.
Schematic Diagram, Typical Inverter Circuit

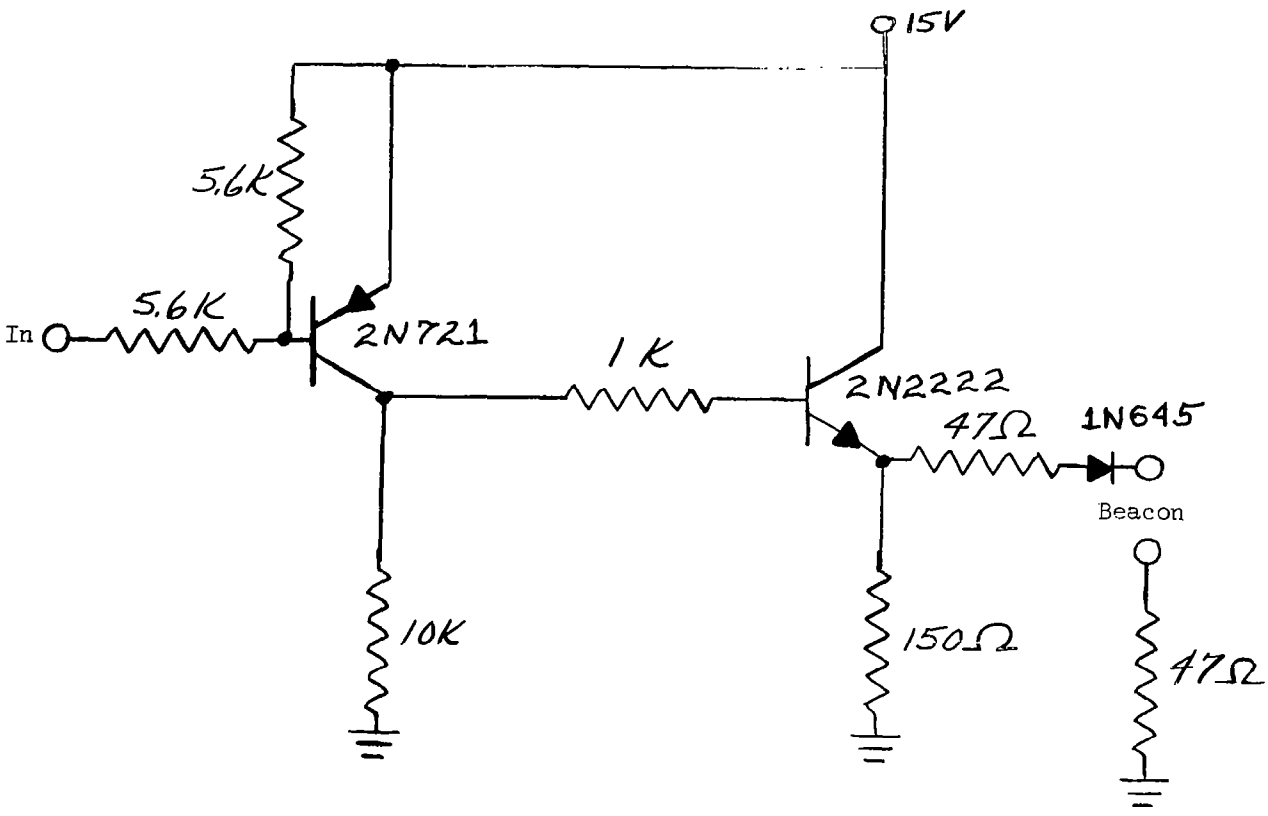


Figure 5-40.
Schematic Diagram, Beacon Driver

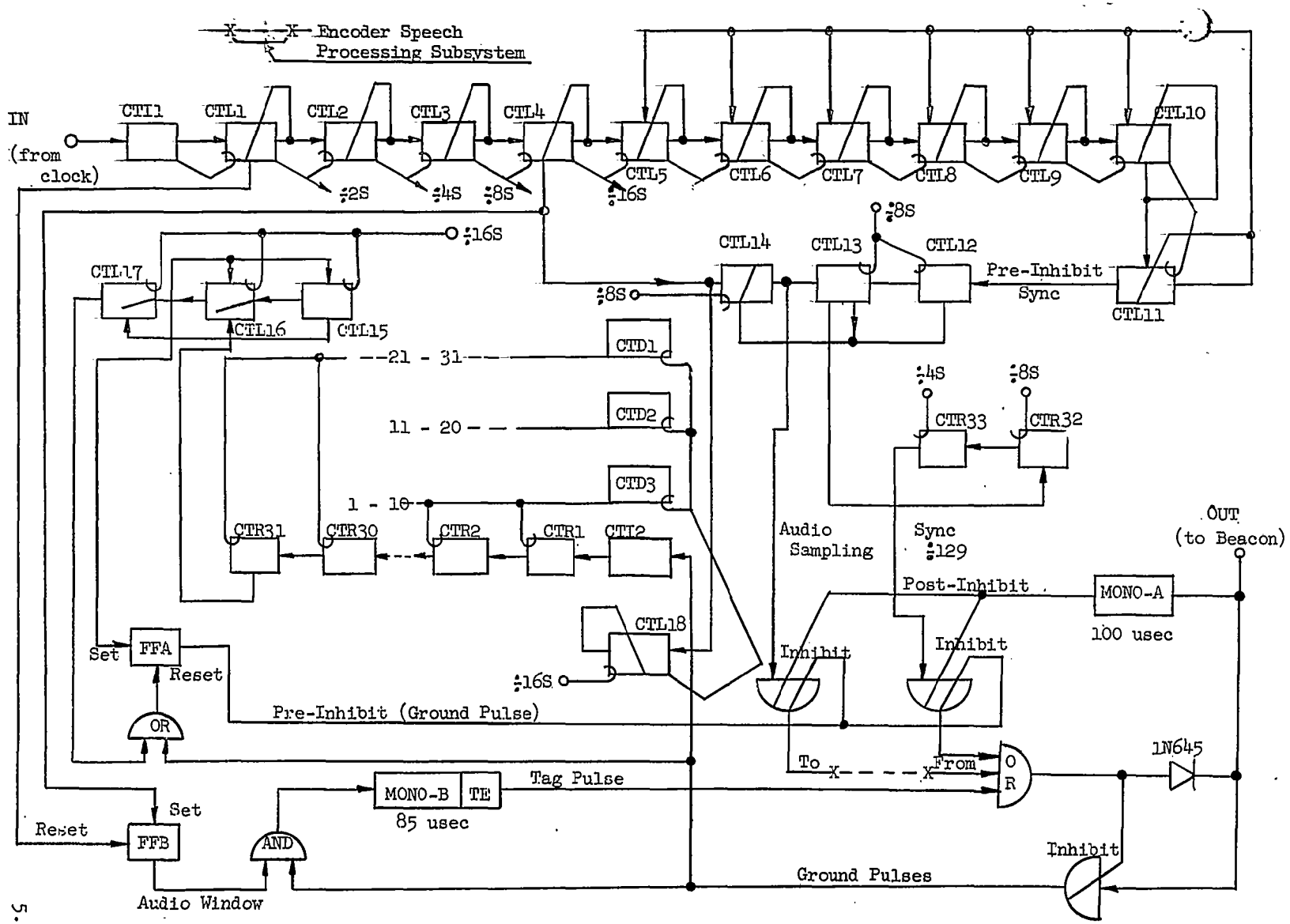


Figure 5-41. Block Diagram, Encoder Sync Subsystem
(Multiple Ground Pulse Train Protection)

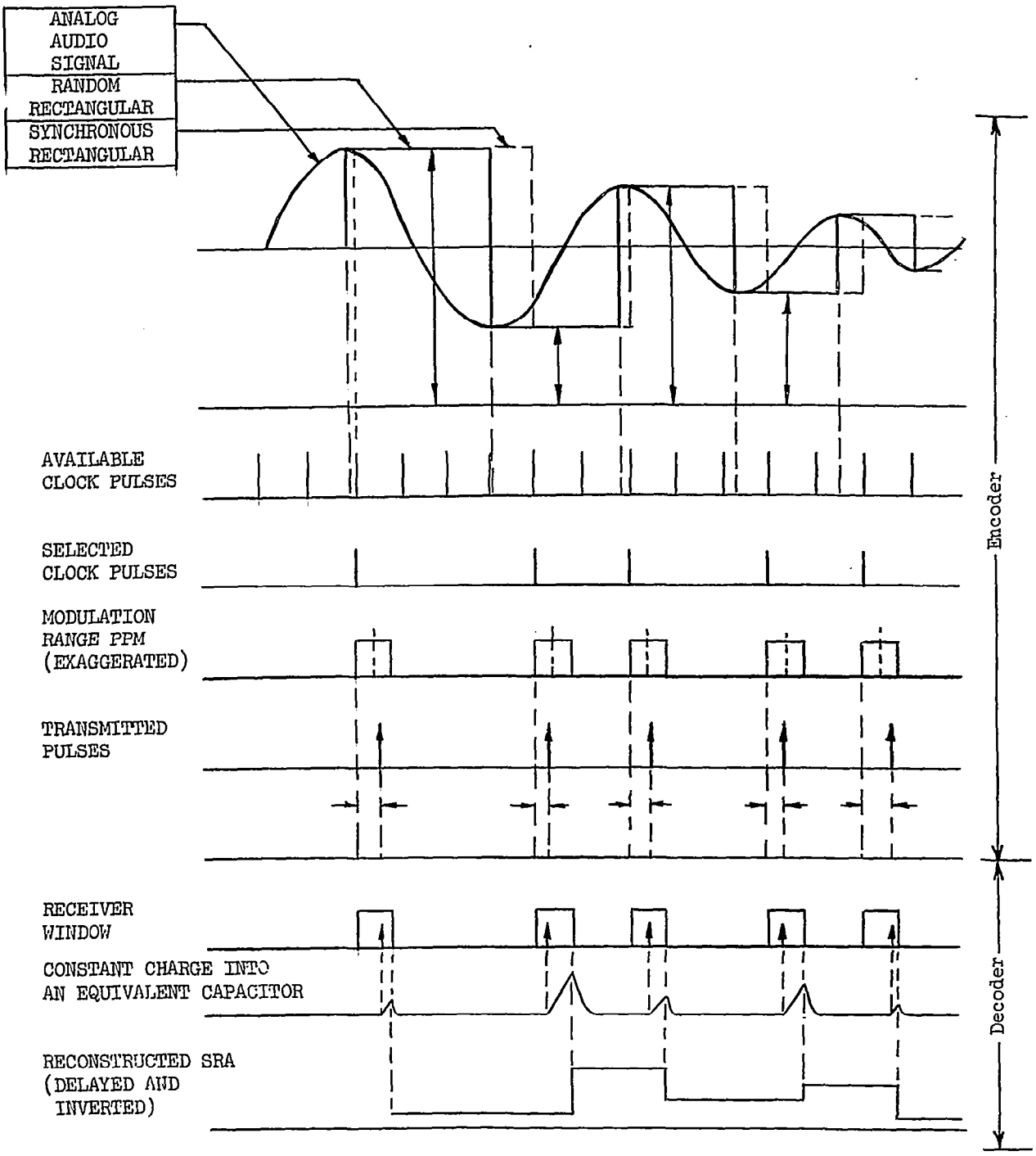


Figure 5-42. Timing and Waveform Diagram, Astrovoice II Encoder/Decoder

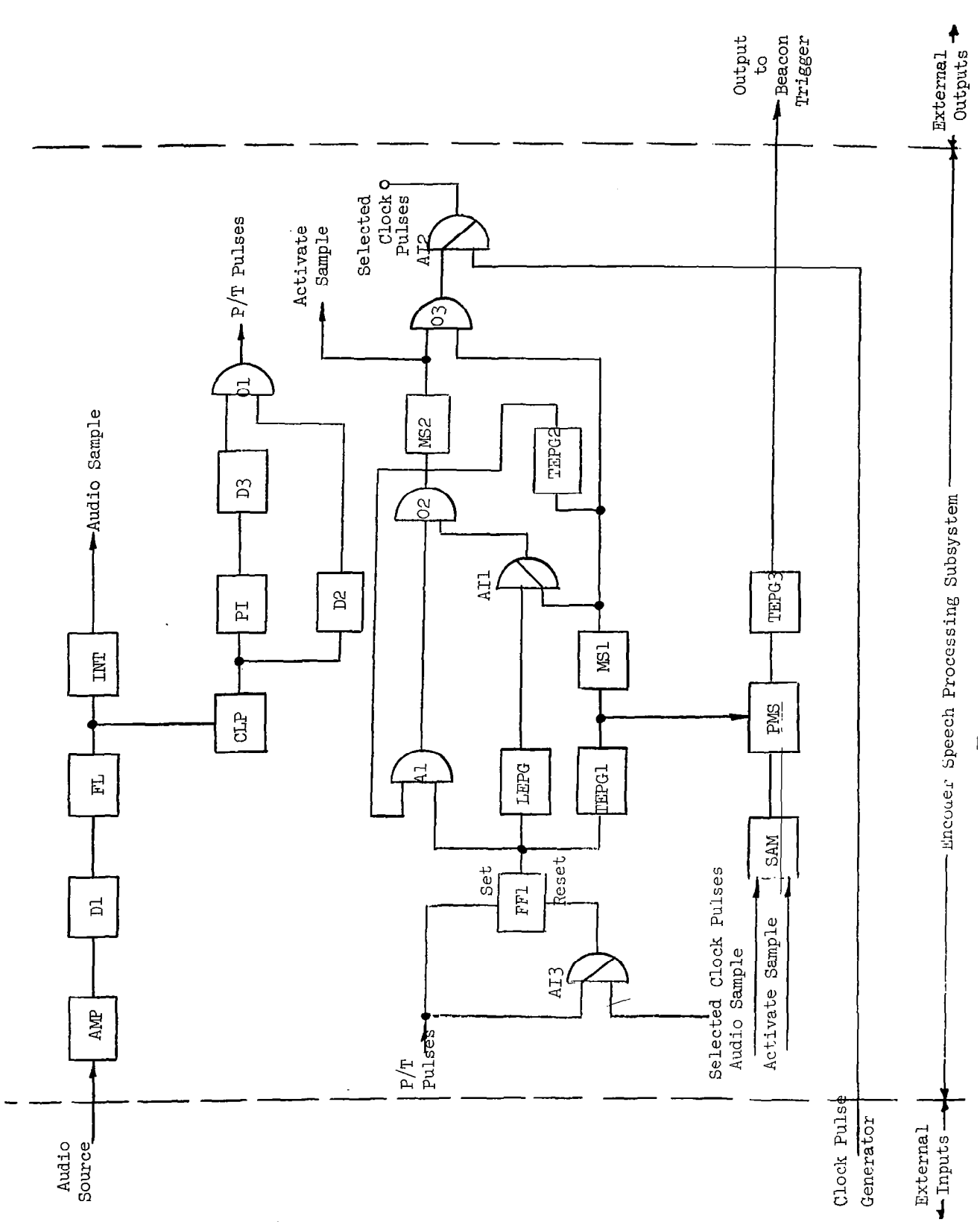


Figure 5-43. Logic Diagram, Encoder Speech Processing Subsystem

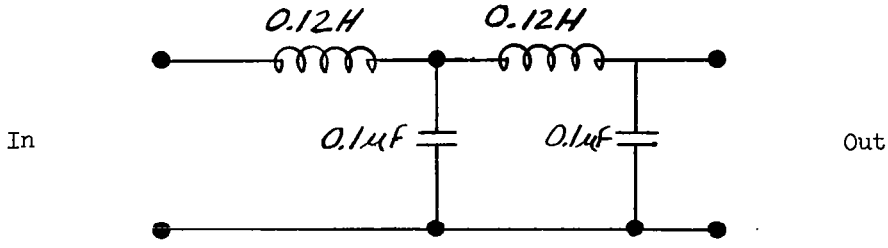


Figure 5-44. Schematic Diagram, Filter

Component Values

	D1	D2	D3
R	5K	10K	10K
C	3300uf	1000pf	1000pf

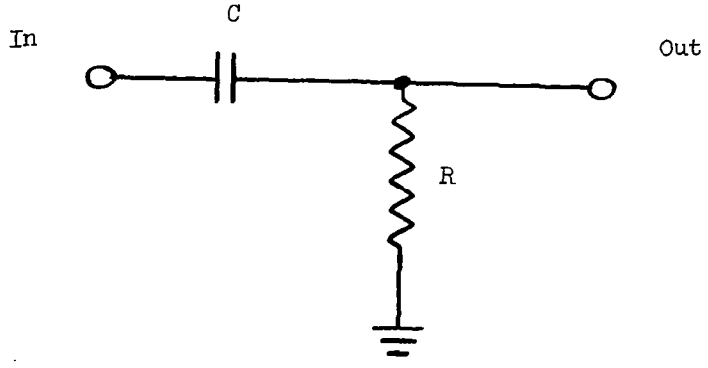


Figure 5-45. Schematic Diagram, Differentiator

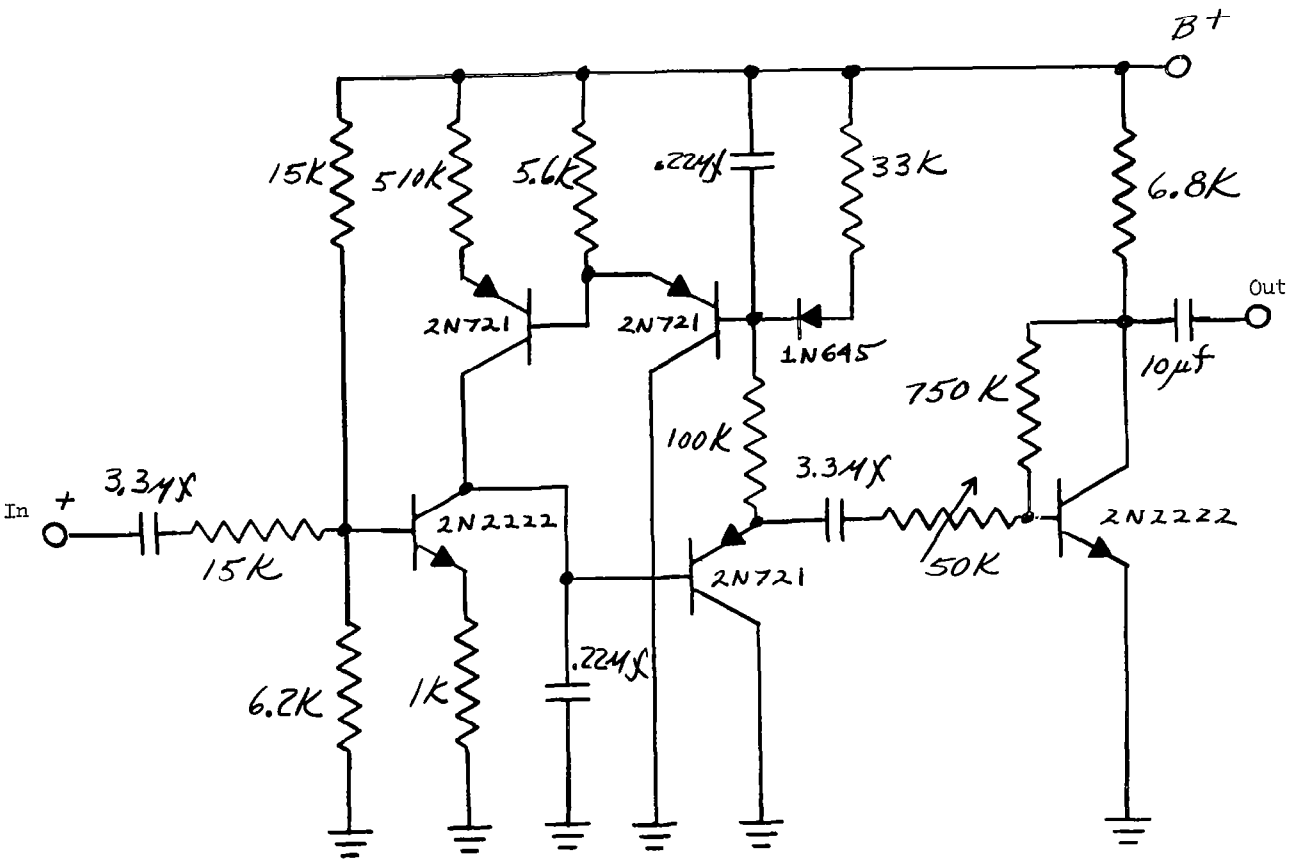


Figure 5-46. Schematic Diagram, Integrator

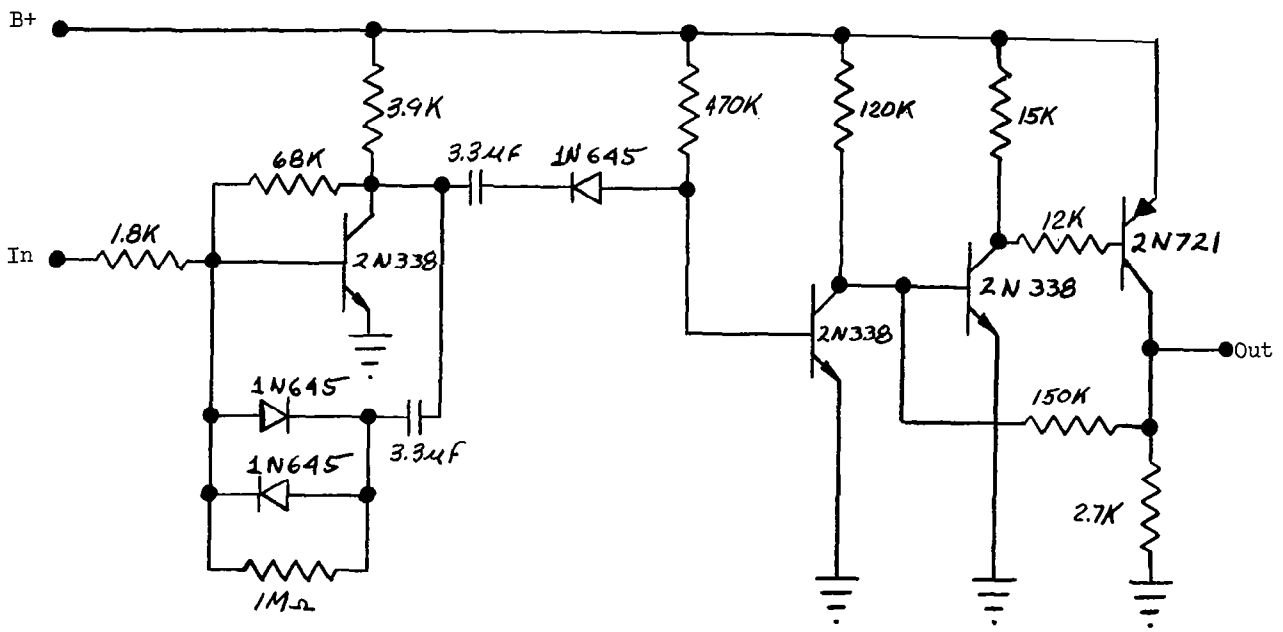


Figure 5-47. Schematic Diagram, Regenerative Clipper

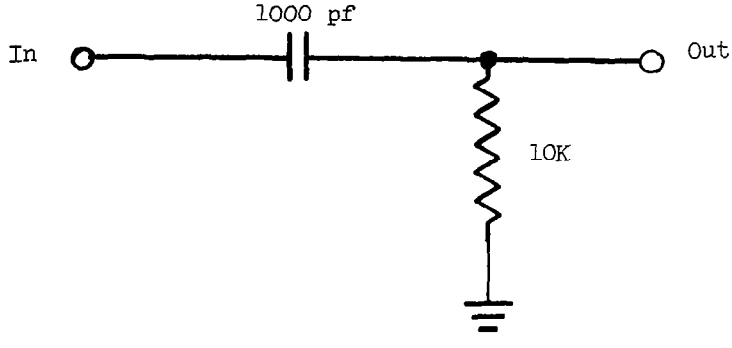


Figure 5-48. Schematic Diagram, Leading Edge Pulse Generator

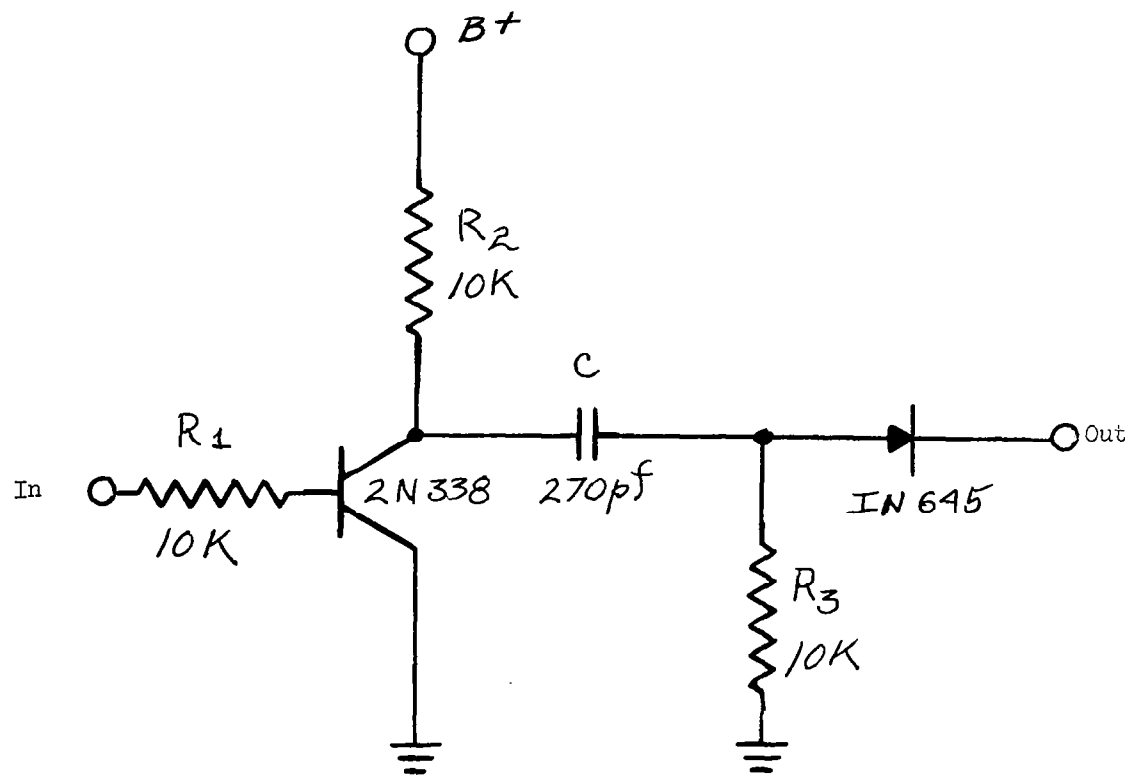


Figure 5-49. Schematic Diagram, Trailing Edge Pulse Generator

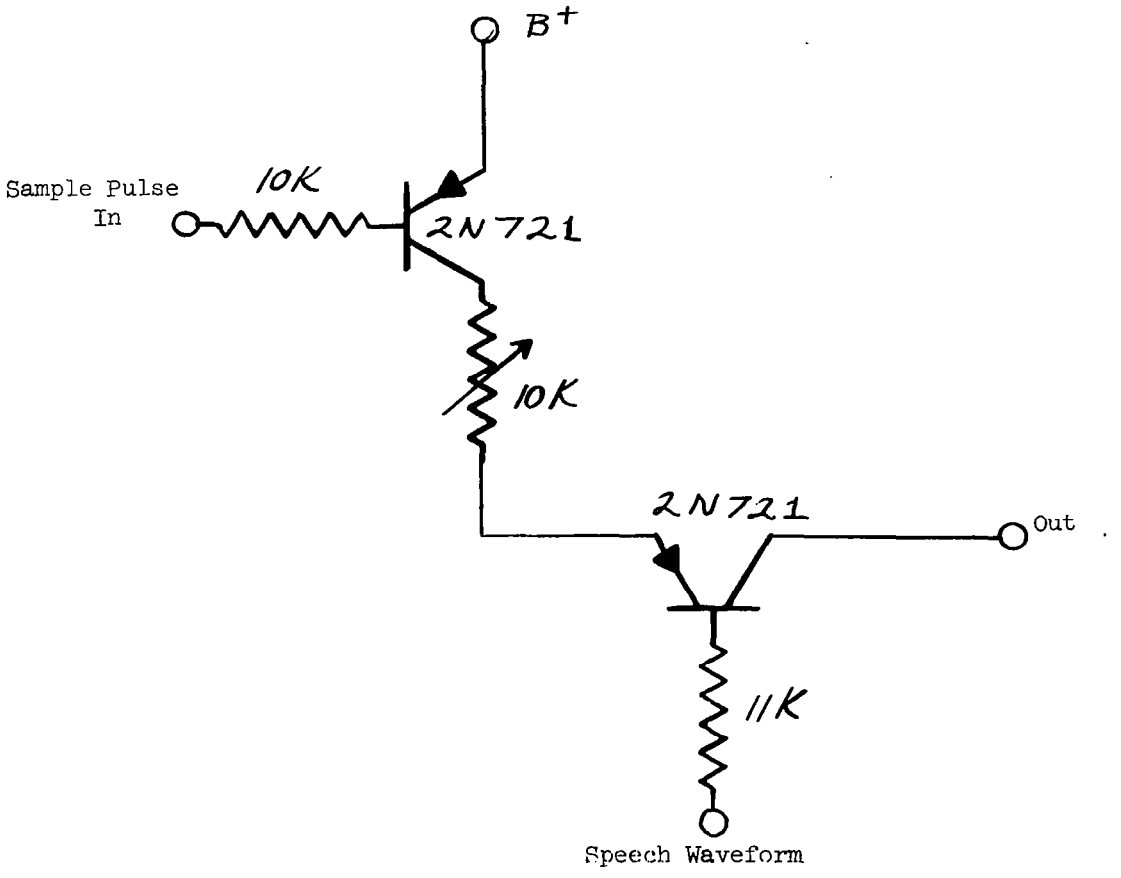


Figure 5-50. Schematic Diagram, Sampler

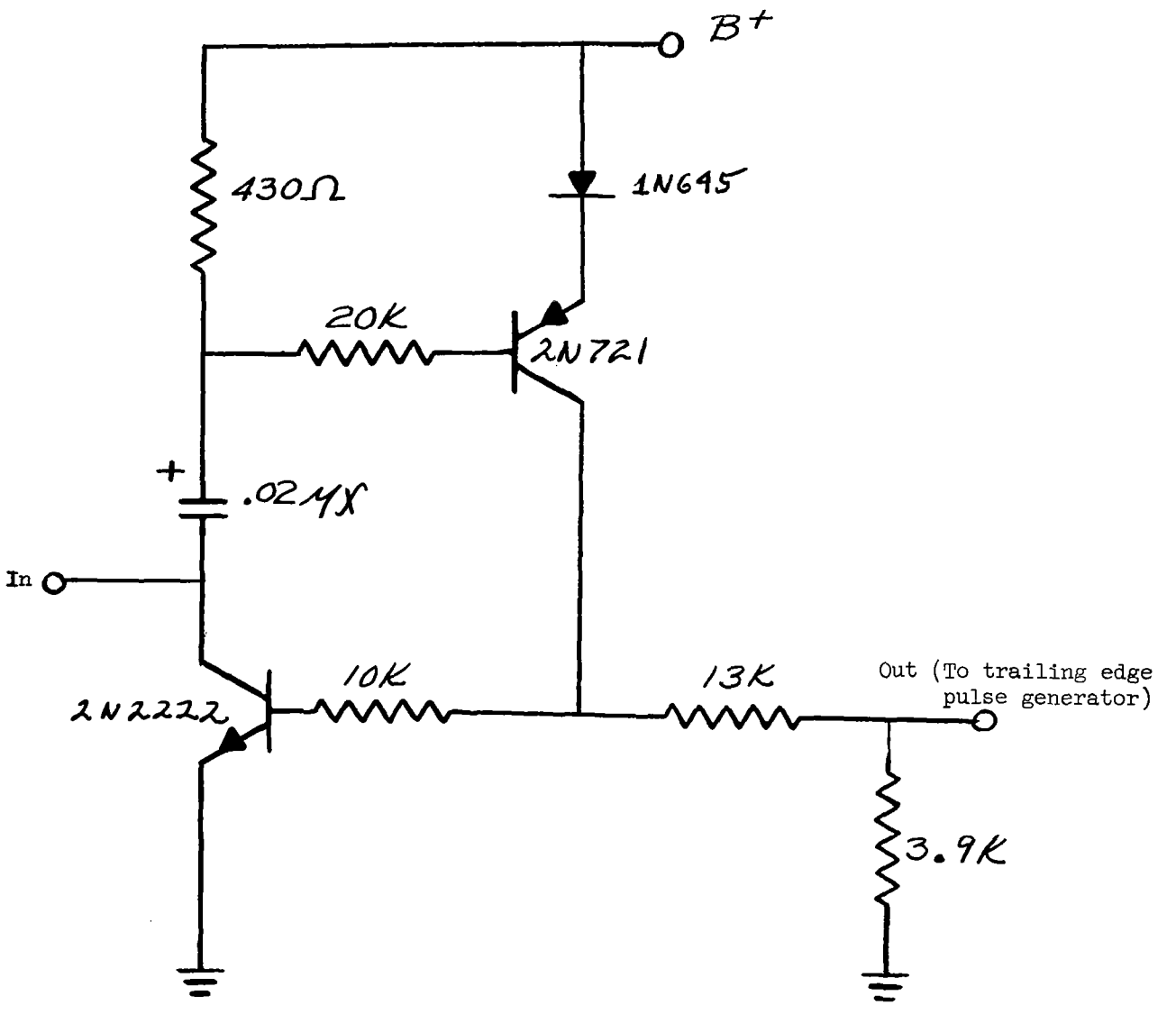


Figure 5-51. Schematic Diagram, Monostable Multivibrator

5.4 DECODER SYSTEM

The Astrovoice decoder system consists essentially of two subsystems-- the decoder synchronization (sync) subsystem (DSS) and the decoder pulse-to-speech demodulation subsystem (PSDS). These are described in paragraphs 5.4.1 and 5.4.2, respectively.

The decoder system, shown in block diagram form on Figure 5-3, enables pulse position modulated (PPM) voice data received from a space vehicle via a tracking radar set to be demodulated. The decoder system is connected to the video detector circuit of the tracking radar set.

As noted in paragraph 5.2, it is assumed for descriptive purposes that the decoder will be operated with a type FPS-16 tracking radar set. Modification of the decoder system to enable it to operate with radar equipment of different characteristics can be accomplished with little difficulty. The principal changes would be in the various dividers and, possibly, in the clock rate.

5.4.1 Decoder Synchronization Subsystem

5.4.1.1 General

In combination, the decoder synchronization subsystem and the decoder pulse-to-speech demodulation subsystem compose the complete Astrovoice II decoder system. The decoder synchronization subsystem (DSS) operates in direct conjunction with the tracking radar equipment as well as with the demodulation subsystem.

5.4.1.2 Design Requirements and Criteria

Major design criteria for the decoder sync subsystem included those imposed by the need to:

Be compatible with the decoder pulse-to-speech demodulation system and with the encoder system.

Meet Astrovoice II decoder system synchronization requirements.

Avoid any interference with the tracking functions of the radar equipment.

These requirements are essentially the same as those for the encoder sync subsystem, described in paragraph 5.3.1.

Operationally, the decoder sync subsystem must:

1. Recognize sync pulses transmitted from the encoder system via the radar beacon and received by the tracking radar set.

2. Use the sync pulses from the encoder system to synchronize operation of the decoder with operation of the encoder system.

3. Prevent sync pulses from the encoder from entering the pulse-to-speech demodulation subsystem.

4. Allow ground pulses, if other than sync pulses, to enter the pulse-to-speech demodulation subsystem. Such ground pulses, if they are received, are suitably tagged prior to transmittal, as described in paragraph 5.3.1.5, to enable the decoder system to identify them. This enables subsequent elimination of the noise interference which they would otherwise produce.

Essentially, therefore, the decoder sync subsystem must be capable of recognizing and properly processing sync pulses.

Three types of pulses appear at the input of the decoder:

5. Ground pulses from the radar tracking equipment. These pulses contain tracking information.

6. Sync pulses from the encoder system. These pulses provide the data required to synchronize operation of the decoder with that of the encoder.

7. Speech pulses from the encoder system. These pulses carry the pulse position modulated (PPM) voice data.

A suitable inhibit interval prevents 'main bang' pulses transmitted by the tracking radar set from interfering with decoder system operation. This interval, approximately 100 μsecs long, is initiated by every pulse transmitted by the radar set.

5.4.1.3 Sync Pulse Recognition

Identification of sync pulses, either those derived from ground pulses or those generated in the encoder (locally generated sync pulses, LGSP's) by the decoder sync subsystem is facilitated by designing the subsystem to take advantage of the fact that such pulses occur at a fixed and known periodic rate. Accordingly, sequential pulses entering the decoder system are tested to determine whether or not they recur at the proper intervals. Those which do are recognized as sync pulses and allowed to enter the decoder sync subsystem. Those which do not are inhibited and prevented from entering the sync subsystem. When the decoder sync subsystem is performing this check, it is defined as being, or operating, in the acquisition mode.

In normal operation an incoming sync pulse will be tested and recognized as such. This and the immediately following sync pulses are then processed in the decoder sync subsystem to synchronize the decoder with the encoder system. Succeeding sync pulses are used to maintain synchronization. When synchronized

in this manner, the decoder is defined as being, or operating, in the in sync mode.

If the series of properly time-spaced sync pulses is interrupted for some reason and the sync pulses fail to recur before the end of a specified interval, the decoder sync subsystem goes out of synchronization, or loses synchronization, and reverts to operation in the acquisition mode.

It should be noted that the term "being, or operating, in the acquisition mode" (or more simply, acquisition mode) and the term "out of synchronization" (or out of sync) are used interchangeably and have the same meaning. Both terms describe the same mode of operation. Usually the term used is that which seems best to emphasize the particular operational aspect being described.

5.4.1.4 Decoder Sync Subsystem Logic and Components

The decoder sync subsystem described in this report was developed, constructed in breadboard model form, and successfully tested. Test results indicated conclusively that the subsystem can be implemented in an operational Astrovoice system. The logic system and components proved fully capable both of synchronizing operation of the decoder system with that of the encoder system and of supplying speech pulses to the demodulation subsystem to enable subsequent processing of pulse position modulated voice data supplied by the encoder system. Tests included those on the decoder sync subsystem operating independently as well as tests in which that subsystem was operated in conjunction with the decoder demodulation subsystem and the complete encoder system.

5.4.1.4.1 General

Decoder sync subsystem operation requires that a train of sync pulses be so defined as to allow:

1. Transition of the subsystem from the acquisition mode to the in sync mode.

2. Transition of the subsystem from the in sync mode to the out of sync (or, as noted in paragraph 5.4.1.3, acquisition) mode.

In general, suitable counters are used to define the sync pulse train. Proper definition requires that three consecutive and correctly spaced pulses be registered in the decoder sync subsystem before synchronization is achieved.

Once synchronization of the decoder system with the encoder system has been established, provision is made for maintaining synchronization. To do this, a gating interval, or window (the 126 window), in the decoder sync subsystem opens automatically just prior to the time at which the next succeeding sync pulse in the sync pulse train would normally be expected to occur. If a sync

pulse is registered during a gating interval, the system remains synchronized. If a sync pulse is not registered during any sixteen (16) consecutive gating intervals, the decoder sync subsystem automatically reverts to operation in the acquisition mode.

5.4.1.4.2 Subsystem Functional Requirements

The decoder sync subsystem is designed to satisfy the following-listed functional requirements:

1. Provide sync pulse gating intervals, or windows.

2. Be capable of operating in the acquisition mode until synchronization is achieved and of reverting to the acquisition mode when synchronization is lost.

3. Recognizing sync pulses and operating in the in sync mode.

The operation of the decoder sync subsystem in meeting these requirements is described in paragraphs 5.4.1.4.2.1, 5.4.1.4.2.2, and 5.4.1.4.2.3, respectively.

The decoder sync subsystem is shown in block diagram form on Figure 5-52.

5.4.1.4.2.1 Sync Pulse Gating

Essentially, five components are used in combination to provide the gating intervals, or windows, used to allow entry of sync pulses into the subsystem. These components, which are similar to corresponding components in the encoder sync subsystem, include a crystal-controlled oscillator (CO), or clock; a regenerative clipper (RC); a divide-by-eight divider (8D); a clock pulse generator (CPG); and a divide-by-128 divider (128D). These series-connected items provide the intervals during which pulses successfully meeting preestablished timing criteria are allowed to enter the decoder sync subsystem. These intervals are usually referred to as the 126 windows. They are produced during the period, approximately 55 μsecs long, that 128D holds a count of 126. The repetition period of the 126 window is approximately 7000 μsecs.

A block diagram indicating the relationships between these components is shown on Figure 5-53.

A sync pulse arriving during the gating interval, while allowed to enter the decoder sync subsystem, is inhibited to prevent its entry into the decoder's pulse-to-speech demodulation subsystem. This assures that only speech pulses (or properly tagged ground pulses--which are subsequently eliminated in the demodulation subsystem in the process of removing noise interference) will be processed, or demodulated, to obtain voice data.

5.4.1.4.2.2 Acquisition Mode

The leading edge (LE) of the 126 window (that is, the beginning of the period during which 128D holds a count of 126) is used to set a flip-flop (FFB) to the ONE state. A logic block diagram illustrating the components used in the decoder sync subsystem when operating in the acquisition mode and indicating the interconnections between these components is shown on Figure 5-54.

FFB is reset to a ZERO state by any pulse which is received during the 126 window. Accordingly, as long as no pulse is received during the 126 window, FFB will remain set. This allows a pulse, called a locally generated miss pulse (LGMP), to trigger a divide-by-16 divider (16D). The LGMP is generated approximately midway through the period during which 128D holds a count of 127. This point in time is generally referred to as time $127\frac{1}{2}$. The divide-by-16 divider is used in defining the subsystem as being in the acquisition mode. 16D is reset to ZERO by every pulse received during the 126 window. The arrangement is such that 16D will lock-up at (that is, retain) a count of 15 if 15 consecutive pulses are not received during the 126 window. Failure to receive the 16th consecutive pulse is not registered in 16D. However, missing such a pulse causes subsystem transition from the in sync mode to the acquisition mode. After the transition, the next pulse received initiates the start of the acquisition cycle (check for reception of three properly spaced pulses).

This approach provides compensation for shifts of up to 0.2 μsecs in the pulse period as a result of Doppler effects. Even if as many as 14 consecutive pulses are blanked out (that is, occur outside of the 126 window) as a result of the Doppler shift, the subsystem will remain in synchronization. The subsystem will lose synchronization in such cases only as a result of gross blanking out of sync pulses. Gross blanking out, as the term is used here, means blanking out of more than 16 sync pulses. The design, therefore, is such that the effects of Doppler shifts do not limit application of the synchronization technique.

5.4.1.4.2.3 In Sync Mode

When 16D holds a count of 15, the LGMP sets a divide-by-four divider (4D) to a ZERO count, thereby allowing any received pulse to reset 8D to a count of ZERO and 128D to a count of 126. A logic block diagram illustrating the components used in the decoder sync subsystem when operating in the sync mode and indicating the interconnections between these components is shown on Figure 5-55.

After being reset to a ZERO count by the LGMP, 4D then begins to count the number of received pulses occurring during the 126 window. If a count of three (3) such consecutive pulses is registered by 4D, 4D locks up at a count of 3, thereby defining the subsystem as being in sync. If however, 4D does not register a count of three such consecutive pulses, it is reset to a count of ZERO by an LGMP. The counting procedure is then repeated following arrival of the next received pulse.

If 4D has reached a count of 3, thereby defining the subsystem as being in sync, it can be reset to a ZERO count only when 16D reaches a count of 15 and holds this count for one ground pulse interval without being reset to ZERO, that is, when the system loses synchronization as a result of missing 16 consecutive sync pulses. Whenever 4D holds a count of 3 and 16D does not hold a count of 15, the subsystem is locked in synchronization and is defined as being in sync.

Synchronization is then maintained by succeeding pulses received during the 126 window. Such pulses maintain synchronization by continually causing 128D to be reset to a count of $126\frac{1}{2}$. This condition provides the gating interval, the 126 window, used to allow entry of the next sync pulse into the decoder sync subsystem.

The description given here is based upon the assumption that ground pulses were used as the source of sync pulses. Provision can be readily made for using other pulses of suitable characteristics (essentially, recurrence at a fixed and known periodic rate). This is accomplished by use of an appropriate clock rate.

5.4.1.4.3 Component Functional Requirements

The following list identifies the essential components required to mechanize the decoder sync subsystem and indicates their principal functions.

1. A clock which provides basic timing data.

2. A divide-by-eight divider (8D) used to provide audio phase 1 and 2 (AØ 1 and AØ 2), and ground phase (GØ) pulses to the subsystem at a rate of approximately 18,176 pps.

3. A divide-by-128 divider (128D) which provides the gating intervals (126 windows) and, in conjunction with other components, locally generated miss pulses (LGMP's) during the 127 window.

4. A divide-by-16 divider (16D) and associated logic circuits used to define the subsystem as being in the acquisition mode.

5. A divide-by-four divider (4D) and associated logic circuits used to define the subsystem as being in the in sync mode.

6. A monostable multivibrator (MONO) used in conjunction with a suitable gating component (the speech pulse gate, SPG) to control entry of speech pulses into the pulse-to-speech demodulation subsystem.

7. A speech pulse gate (SPG) which prevents pulses other than speech pulses from entering the pulse-to-speech demodulation system.

8. A flip-flop (FFA) used in defining the system as being in the acquisition mode.

9. A flip-flop (FFB) used to control generation of locally generated miss pulses (LGMP's).

10. A gate, the received pulse gate (RPG), which directs received pulses to appropriate portions of the decoder sync subsystem.

11. A gate, the locally generated miss pulse gate (LGMPG), used to control the flow of LGMP's in the subsystem.

5.4.1.4.4 Component Operation

The major components of the decoder sync subsystem operate as follows. Logic interconnections between these components are shown on Figure 5-52. As noted previously (paragraph 5.3.1.7.4), in the interest of conserving design effort certain of the major components (crystal-controlled oscillator, regenerative clipper, clock pulse generator, and the divide-by-eight and divide-by-128 dividers) have been so designed that they can be used alternatively in either the encoder or decoder sync subsystems with only slight modifications.

A summary of the conditions under which various components are set, reset, or triggered is given on Table 5-2.

5.4.1.4.4.1 Clock

For a description of the clock, or crystal-controlled oscillator (CO), see paragraph 5.3.1.7.4.1.

5.4.1.4.4.2 Regenerative clipper

For a description of the regenerative clipper (RG), see paragraph 5.3.1.7.4.2.

5.4.1.4.4.3 Divide-by-Eight Divider

The divide-by-eight divider (8D) is essentially the same in design as the divide-by-eight divider used in the encoder sync subsystem. For a description of 8D, see paragraph 5.3.1.7.4.3.

5.4.1.4.4.4 Clock Pulse Generator

The clock pulse generator (CPG) is essentially the same in design as the clock pulse generator used in the encoder sync subsystem. For a description of the CPG, see paragraph 5.3.1.7.4.4.

Table 5-2

Summary, Decoder Sync Subsystem Component

Set, Reset, and Trigger Conditions

Flip-Flop A (FFA)	
Set	Reset
By LGMP When 4D does not hold a count of 3 (during transition states of 4D--0, 1, 2) OR After the 15th consecutive pulse is missed (during 15W)	By next received pulse Immediately after being set OR During 126W
Flip-Flop B (FFB)	
Set	Reset
By leading edge of 126W	By next received pulse During 126W OR When enabled by FFA
Divide-by-Four Divider (4D)	
Triggered	Reset
By received pulses During 126W AND If in a transition state (0, 1, 2)	Only by LGMP During transition states (0, 1, 2) OR After the 15th consecutive pulse is missed (during 15W)

Table 5-2 (Cont.)

Divide-by-Sixteen Divider (16D)	
Triggered	Reset
By LGMP If in a transition state (0, 1, 2,..,14)	By received pulses During 126W OR When enabled by FFA

5.4.1.4.4.5 Divide-by-128 Divider

The divide-by-128 divider (128D) is essentially the same in design as the divide-by-128 divider used in the encoder sync subsystem. For a description of 128D, see paragraph 5.3.1.7.4.5. The principal differences are in the number of windows provided and in the use of the output pulses. 128D as used in the decoder sync subsystem does not provide a 124 window, and the 126 and 127 window output pulses are used as follows:

> 126W pulses are sent to the received pulse gate (RPG) and they are also sent to the 126 window inverter (126W Inv) where they are inverted and sent to the speech pulse gate (SPG), the received pulse gate (RPG), and flip-flop B (FFB).
>
> 127W pulses are sent to the locally generated miss pulse gate (LGMPG).

In addition, 128D as used in the decoder sync subsystem is reset by the output of the RPG instead of by sync pulses from a counter reset circuit.

5.4.1.4.4.6 126-Window Inverter

The 126-window inverter (126W Inv) receives input signals from 128D during the 126 window and provides inverted pulses to the speech pulse gate (SPG), received pulse gate (RPG), and flip-flop B (FFB). The circuit used is shown schematically on Figure 5-56. The circuit is similar to that described in paragraph 5.3.1.7.6.11 and shown schematically on Figure 5-39.

5.4.1.4.4.7 Speech Monostable Multivibrator

The speech monostable multivibrator (MONO) receives audio phase 2 (AØ 2) pulses from the clock pulse generator (CPG) and provides output signals to the speech pulse gate (SPG). Its basic function is to provide a suitable gating interval after each audio phase pulse. The gating interval (based on the period of the multivibrator--approximately 14 μsecs) is long enough to enable all speech pulses to enter the pulse-to-speech demodulation subsystem via the SPG. The interval will allow entry of pulses delayed up to the maximum delay (14 μsecs) introducted in the encoder system when pulse position modulating voice data. Pulses occurring outside of the interval are not required for the demodulation process and they are, therefore, prevented from entering the demodulation subsystem. The multivibrator circuit is shown schematically on Figure 5-57. It is in many respects similar to the multivibrator described in paragraph 5.3.1.7.6.7 and shown schematically on Figure 5-35.

5.4.1.4.4.8 Speech Pulse Gate

The speech pulse gate receives inputs in the form of audio phase 2 (AØ 2) pulses from the divide-by-128 divider (128D) via the speech monostable

multivibrator (MONO), output signals from the 126-window inverter (126W Inv), and received pulses from the received pulse gate (RPG). When MONO is ON (that is, producing a ZERO output level) and the 126W Inv is OFF (that is, producing a ZERO output level), received pulses can pass through SPG to the demodulation subsystem. This arrangement inhibits all pulses received during 126W or received outside of the gating interval (14 μsecs) provided by MONO. The circuit used is shown schematically on Figure 5-58.

5.4.1.4.4.9 Flip-Flop A

Flip-flop A (FFA) is used in defining operation of the decoder sync subsystem in the acquisition mode. FFA is set to a ONE state by the output of the locally generated miss pulse gate (LGMPG). It is reset to a ZERO state by the output of the received pulse gate (RPG). That is, FFA is set to a ONE state under the conditions expressed in the following logic statement which also presents the conditions under which the LGMPG output signal is produced (insofar as FFA is concerned):

$$(\text{FFA}) = \left[(\text{G}\emptyset)\ (\text{FFB})(127\text{W})\right]\left[(15\text{W}) + (\overline{3\text{W}})\right]$$

and it is reset to a ZERO state under the conditions expressed in the following logic statement:

$$(\overline{\text{FFA}}) = \left[(\text{FFA}) + (126\text{W})\right] \quad (\text{Received Pulse}).$$

When FFA is set to the ONE state, its output is applied to the received pulse gate where it is used in conjunction with received pulses to reset both the divide-by-16 divider (16D) to a ZERO count and the divide-by-128 divider (128D) to a count of $126\frac{1}{2}$ (a point midway through the period during which 128D holds a count of 126). These conditions may be expressed in the form of a logic statement as:

$$(\text{FFA})(\text{Received Pulses}) = (16\text{D to ZERO})(128\text{D to } 126\tfrac{1}{2}).$$

The flip-flop circuit is shown schematically on Figure 5-59. It is similar to that of the set-reset type bistable multivibrator described in paragraph 5.3.1.7.6.4 and shown schematically on Figure 5-32.

5.4.1.4.4.10 Flip-Flop B

Flip-flop B (FFB) is used in controlling generation of locally generated miss pulses (LGMP's). It is set to a ONE state by the leading edge (LE) of the 126 window (126W) waveform and reset to a ZERO state by the output of the received pulse gate (RPG). These conditions, expressed in logical statement form and, in the reset case, expanded to include the conditions under which RPG provides an output signal to FFB are:

$$(\text{FFB}) = (\text{LE } 126\text{W})$$

$$(\overline{\text{FFB}}) = \left[(\text{FFA}) + (126\text{W})\right] \quad (\text{Received Pulse}).$$

Insofar as FFB is concerned, locally generated miss pulses (LGMP's) are produced by ground phase (GØ) pulses when FFB is set and the divide-by-128 divider (128D) holds a count of 127. That is, for FFB:

$$(\text{LGMP}) = (\text{G}\emptyset)(\text{FFB})(\text{127W}).$$

The flip-flop circuit is shown schematically on Figure 5-60. It is similar to that of the set-reset type bistable multivibrator described in paragraph 5.3.1.7.6.4 and shown schematically on Figure 5-32.

5.4.1.4.4.11 Divide-by-16 Divider

The divide-by-16 divider (16D) is used to count consecutive locally generated miss pulses (LGMP's). A self-locking feature is provided. 16D's output goes to the LGMP gate (LGMPG) via the 15-window inverter (15W Inv). Registration in 16D of a count of 15 consecutive LGMP's signals transition of the decoder sync subsystem from the in sync mode to the acquisition, or out of sync, mode. Counting is triggered by input pulses from the LGMPG. 16D is reset to ZERO by the output of the received pulse gate (RPG). The following logic statement indicates the conditions under which 16D is reset to a ZERO count and the RPG output is produced.

$$(\text{16D reset to ZERO}) = (\text{Received Pulse}) \left[(\text{FFA}) + (\overline{\text{126W}})\right]$$

16D is self-locking in that it provides the 15 window (15W) signal to the LGMPG which in turn produces the pulse used to trigger counting in 16D. This may be expressed in logic statement form as:

$$(\text{Trigger Pulse}) = (\text{LGMP})(\overline{\text{15W}})$$

where LGMP is produced by ground phase (GØ 1) pulses when flip-flop B (FFB) is set and the divide-by-128 divider (128D) holds a count of 127. That is:

$$(\text{LGMP}) = (\text{G}\emptyset)(\text{FFB})(\text{127W}).$$

The divider is composed of 4 serial bistable multivibrators, or binary dividers, interconnected logically as shown on Figure 5-61. The circuit of one stage of the divider is shown schematically on Figure 5-62. The multivibrators used in 16D are the triggered type A bistable multivibrators described in paragraph 5.3.1.7.6.5 and shown schematically on Figure 5-33. Negative outputs are used, thus 15_{10} is represented by a 0000_2 output and 0_{10} is represented by a 1111_2 output instead of by 1111_2 and 0000_2 outputs, respectively.

5.4.1.4.4.12 Divide-by-Four Divider

The divide-by-four divider (4D) is used to count consecutive received pulses occurring in the 126 window when the subsystem is in the acquisition mode. A self-locking feature is provided. 4D's output goes to the locally generated miss pulse gate (LGMPG) and the received pulse gate (RPG) via the 3-window

inverter (3W Inv) and 3 window inhibit gate (3W Inh). Registration in 4D of 3 consecutive received pulses from the RPG signals transition of the decoder sync subsystem from the acquisition, or out of sync, mode to the in sync mode. Counting is triggered by input pulses from the received pulse gate (RPG). 4D is reset to a ZERO count by locally generated miss pulses occurring when either 4D does not hold a count of 3 or the divide-by-16 divider (16D) holds a count of 15. The following logic statement indicates the conditions under which 4D is reset:

$$(\text{4D reset to ZERO}) = \left[\overline{(3W)} + (15)\right] \quad (\text{LGMP}).$$

4D is self-locking in that the 3 window (3W) associated with 4D inhibits output pulses from locally generated miss pulse gate (LGMP) and received pulse gate (RPG). These pulses, when not inhibited, are used in the received pulse gate (RPG) to trigger counting by 4D. The divider is composed of 2 serial bistable multivibrators, or binary dividers, interconnected logically as shown on Figure 5-63. The circuit of one stage of the divider is shown schematically on Figure 5-62. The multivibrators used in 4D are the triggered type A bistable multivibrators described in paragraph 5.3.1.7.6.5 and shown schematically on Figure 5-33. Negative outputs are used, thus 3_{10} is represented by a 00_2 output and 0_{10} is represented by a 11_2 output instead of by 11_2 and 00_2 outputs, respectively.

5.4.1.4.4.13 15-Window and 3-Window Inverters

The 15-window and 3-window inverters (15W Inv and 3W Inv, respectively) are used to:

Invert, from a ZERO to a ONE, the output level signal produced during the window period with which each inverter is associated. This facilitates certain logic applications of the signal.

Provide a voltage step-down. The output voltage of the divider with which the inverter is associated is reduced since the ZERO level output of the inverter is <u>not</u> at ground potential.

The 15-window inverter (15W Inv) receives inputs from the divide-by-16 divider (16D) when 16D holds a count of 15. Its output goes to the locally generated miss pulse gate (LGMPG). The 3-window inverter (3W Inv) receives inputs from the divide-by-4 divider (4D) when 4D holds a count of 3. Its output goes to the 3-window inhibit gate (3W Inh) associated with 4D. The circuit is shown schematically on Figure 5-64. It is similar to the inverter circuit described in paragraph 5.3.1.7.6.11 and shown on Figure 5-39.

5.4.1.4.4.14 3-Window Inhibit Gate

The 3-window inhibit gate (3W Inh) is used to provide self-locking capability for the divide-by-four divider (4D). It receives its input from the 3-window inverter (3W Inv) and provides an output to the locally generated miss pulse gate (LGMPG) and the received pulse gate (RPG). When 4D holds a count of 3

the output from 3W Inv is shunted to ground, thereby preventing further triggering of 4D by pulses from the received pulse gate (RPG) where the 4D output pulses are used to trigger 4D. The circuit is shown schematically on Figure 5-65.

5.4.1.4.4.15 Received Pulse Gate

The received pulse gate (RPG) provides means for directing received pulses to appropriate portions of the decoder sync subsystem. Received pulses are directed to the speech pulse gate (SPG) when 128D does not hold a count of 126; to the divide-by-8 divider to reset that divider to a count of 4; to the divide-by-16 divider (16D), the divide-by-128 divider (128D), flip-flop A (FFA), and flip-flop B (FFB) when FFA is set to a ONE state or 128D holds a count of 126; and to the divide-by-4 divider (4D) when 4D does not hold a count of 3 and the divide-by-128 divider (128D) holds a count of 126. The circuit is shown in schematic diagram form on Figure 5-66. It consists essentially of a combination of AND gates and inverters of the types described in paragraphs 5.3.1.7.6.8 and 5.3.1.7.6.11 and shown on Figures 5-36 and 5-39, respectively.

5.4.1.4.4.16 Locally Generated Miss Pulse Gate

The locally generated miss pulse gate (LGMPG) provides means for generating locally generated miss pulses and for directing them to appropriate portions of the decoder sync subsystem. LGMP's are generated in response to ground phase (GØ) pulses when flip-flop B (FFB) is set to a ONE state and the divide-by-128 divider (128D) holds a count of 127 and the divide-by-16 divider (16D) holds a count of 15. LGMP's are directed to 16D to initiate, or trigger, counting. In addition, when the divide-by-4 divider (4D) does not hold a count of 3 or the divide-by-16 divider (16D) holds a count of 15, LGMP's are sent to flip-flop A (FFA) to set it to a ONE state and to the divide-by-4 divider (4D) to reset 4D to a count of ZERO. The circuit is shown schematically on Figure 5-67. It consists essentially of a combination of AND gates and inverters of the types described in paragraphs 5.3.1.7.6.8 and 5.3.1.7.6.11 and shown on Figures 5-36 and 5-39, respectively.

5.4.1.4.5 Basic Encoder/Decoder Sync Subsystem Circuits

The basic circuits used in mechanizing the decoder sync subsystem logic are similar to those described in paragraph 5.3.1.7.6 and its subparagraphs.

5.4.1.4.6 Logic States

Descriptions of the various states of the decoder sync subsystem logic and of the state of individual components at each state of the decoder sync subsystem logic follow. The logic flow diagram shown on Figure 5-68 indicates basic interrelationships between the various logic states.

STATE I — No pulses yet received or the 16th consecutive pulse was missed while 128D holds a count of 126.

a. Flip-flop A (FFA) is set to a ONE state.

b. Flip-flop B (FFB) is set to a ONE state.

c. The divide-by-16 divider (16D) holds a count of 15.

d. The divide-by-4 divider (4D) holds a count of ZERO.

e. The divide-by-8 and divide-by-128 dividers (8D and 128D) are free running.

f. The subsystem is in the acquisition mode.

STATE II — The first pulse arrives or the next pulse arrives after the 16th consecutive pulse was missed while 128D held a count of 126.

a. The divide-by-8 divider (8D) is set to a count of 4.

b. The divide-by-128 divider (128D) is set to a count of 126.

c. The divide-by-4 divider (4D) remains set at a count of ZERO.

d. Flip-flop A is reset to a ZERO state.

e. Flip-flop B is reset to a ZERO state.

f. The divide-by-16 divider (16D) is set to a count of ZERO.

g. The subsystem is in the acquisition mode.

STATE III — Testing for a sync pulse.

STATE III-1 — Three consecutive pulses do not arrive while 128D holds a count of 126 after the subsystem has been in State II.

a. Flip-flop B (FFB) remains set during and after the time 128D retains a count of 126. This enables generation of an LGMP.

b. The divide-by-16 divider (16D) is at a count other than that of 15 and is counting.

c. The divide-by-4 divider (4D) is reset to a count of ZERO by the LGMP. Until reset it was at a count other than that of 3 and was counting.

d. Flip-flop A (FFA) is set to a ONE state.

e. The next received pulse causes the subsystem to revert to State II.

STATE III-2 Three consecutive pulses arrive while 128D holds a count of 126 after the subsystem has been in State II.

a. Flip-flop B (FFB) is reset to a ZERO state by the pulses.

b. Flip-flop A (FFA) remains in the ZERO state.

c. The divide-by-16 divider (16D) remains set at a count of ZERO.

d. The divide-by-4 divider (4D) is locked at a count of 3 and does not, therefore, re-cycle in response to further received pulses.

e. The decoder is defined as being in sync. 16 consecutive pulses occurring while 128 holds a count of 126 must be missed before the subsystem loses sync and is redefined as being out of sync, or in the acquisition mode.

NOTE: The 16th pulse missed is not counted by the divide-by-16 divider (16D).

STATE IV The subsystem is in sync but pulses are being missed while 128D holds a count of 126 after the subsystem has been in State II.

STATE IV-1 15 consecutive pulses have not yet been missed and no pulse has yet arrived while 128D holds a count of 126.

Same as State III-2 except that:

1. Flip-flop B (FFB) is not reset to a ZERO state.

2. The divide-by-16 divider (16D) counts in response to LGMP's.

STATE IV-2 15 consecutive pulses have not yet been missed and a pulse arrives while 128D holds a count of 126.

a. The divide-by-16 divider is reset to a count of ZERO.

b. The subsystem automatically reverts to State III-2.

STATE IV-3 15 consecutive pulses have been missed while 128D holds a count of 126.

a. The divide-by-16 divider (16D) is set to a count of 15 by LGMP.

b. Flip-flop A (FFA) remains reset to a ZERO state.

c. Flip-flop B (FFB) is set to a ONE state.

d. The divide-by-4 divider (4D) remains set at a count of 3.

e. After the 16th consecutive missed pulse, the subsystem reverts to State I.

5.4.1.4.7 Timing Diagrams

Timing diagrams illustrating operation of various decoder sync subsystem components under stated received pulse formats are presented on Figures 5-69, 5-70, 5-71, and 5-72, as follows:

Figure 5-69	Missing Every Other Pulse
Figure 5-70	Ground Pulse Frequency Low
Figure 5-71	Ground Pulse Frequency High
Figure 5-72	Sync Pulses and Random Audio (Out of Sync) Pulses.

A diagram illustrating timing relationships between various functions of the encoder and decoder systems is shown on Figure 5-42.

5.4.2 Decoder Pulse-to-Speech Demodulation Subsystem

The decoder pulse-to-speech demodulation subsystem (PSDS) operates in conjunction with the decoder sync subsystem to produce speech waveforms in response to pulse position modulated (PPM) speech pulses received from a spacecraft via a tracking radar set.

5.4.2.1 General

The decoder pulse-to-speech demodulation subsystem is designed to:

1. Be compatible with the decoder sync subsystem.
2. Avoid any interference with the tracking function of the tracking radar equipment.
3. Accept pulse position modulated voice data.
4. Produce waveforms which are facsimiles of the speech waveforms applied to the audio input stage of the encoder system.

The decoder pulse-to-speech demodulation subsystem was developed, constructed in breadboard model form, and thoroughly tested--both alone and when operated in conjunction with the decoder sync subsystem and the encoder system. All design requirements were successfully met.

Test results indicate that the design can be implemented in an operational decoder pulse-to-speech demodulation subsystem for Astrovoice system applications.

5.4.2.2 Decoder Pulse-to-Speech Demodulation Subsystem Logic and Components

5.4.2.2.1 General

The decoder pulse-to-speech demodulation subsystem is designed to convert speech pulses into output waveforms which are rectangular facsimiles of the audio input waveforms entering the encoder system. The speech pulses are pulse position modulated (PPM) in time with respect to pulses produced at a stable rate by a clock (clock pulses). The speech pulses reach the decoder pulse-to-speech demodulation subsystem from the encoder system via a radar beacon on the spacecraft and the video detector of a ground-based tracking radar set.

A logic diagram of the subsystem is shown on Figure 5-73.

5.4.2.2.2 Subsystem Functional Requirements

Analysis of design requirements for a decoder pulse-to-speech demodulation

subsystem capable of processing pulse position modulated signals indicated that the system must perform the following-listed basic functions.

1. Compare pulse position modulated speech pulses received from a tracking radar set's video detector with pulses in a locally generated train of clock pulses to determine the actual time-modulation introduced in the speech pulses by the encoder speech processing subsystem.

2. Derive amplitude information from the time modulation data.

3. Construct from the amplitude data rectangular-type waveforms which are facsimiles of the speech waveforms applied to the audio input of the encoder system. The facsimile waveforms, from which intelligible voice data can be extracted, are generally referred to in this report as synchronous rectangular audio (SRA) waveforms.

5.4.2.2.3 Component Functional Requirements

The following list identifies and indicates the principal functional requirements of the essential components required to mechanize the decoder pulse-to-speech demodulation subsystem logic. The components listed are shown on the subsystem logic diagram, Figure 5-73.

1. A clock pulse generator (CPG) is used as the source of locally generated clock pulses. The clock pulse generator is essentially the same in design as the clock pulse generator used in the encoder and decoder sync subsystems. The circuit is described in paragraph 5.3.1.7.6.3 and shown on Figure 5-31.

2. Flip-flop 1 (FF1) is a set-reset type bistable multivibrator which provides two complementary outputs, FF1 and $\overline{FF1}$. These are used to perform logic functions. The flip-flop circuit is similar to that described in paragraph 5.3.1.7.6.4 and shown in schematic diagram form on Figure 5-32.

3. Flip-flop 2 (FF2) is a triggered bistable multivibrator which provides two complementary outputs, FF2 and $\overline{FF2}$. These are used to perform logic functions. The flip-flop circuit is similar to that described in paragraph 5.3.1.7.6.5 and shown in schematic diagram form on Figure 5-33.

4. A monostable multivibrator (MS1) is used to generate an output voltage for a finite period of time following receipt of an appropriate input, or triggering, signal. At the end of that time the output voltage returns to the quiescent state level. The multivibrator output signal is used in conjunction with a trailing edge pulse generator (TEPG2) to reset flip-flop 1 to a ZERO state, and, in conjunction with an AND gate (A1) and with incoming signals from the radar set's video detector, to set that same flip-flop to a ONE state. The circuit used for the multivibrator is essentially the same as that described in paragraph 5.3.1.7.6.7 and shown schematically on Figure 5-35.

5. Two constant current charge circuits (CHG1 and CHG2) are used. Each provides a constant current charge to an associated capacitor (C1 and C2, respectively, as shown on Figure 5-73). The capacitor is charged during the time interval during which a signal is present at the circuit's input terminal. The charge circuit is such that it allows the charge to be held for a relatively long period of time (on the order of 0.5 sec) even after termination of the input signal. The circuit is shown schematically on Figure 5-74.

6. Two discharge circuits (DCG1 and DCG2) are used. Each provides an essentially infinite input impedance to a capacitor (C1 and C2, respectively) attached to the discharge circuit's output terminal whenever no signal is applied to the circuit's input terminal. When the specified signal is applied to the circuit's input terminal, however, the circuit presents an appropriate resistance to the capacitor. This arrangement enables the associated capacitor to be discharged prior to the arrival of the next clock pulse. The circuit is shown schematically on Figure 5-75.

7. A phase inverter (PI) inverts the output signal produced by the decoder pulse-to-speech demodulation subsystem, thereby providing a synchronous rectangular audio facsimile waveform at the decoder system's output terminals. The circuit is similar to that described in paragraph 5.3.1.7.6.11 and shown schematically on Figure 5-39.

8. Two trailing edge pulse generators (TEPG1 and TEPG2) are used. Each is used to produce a pulse coincident with the trailing edge of a square wave pulse. The circuit is similar to that used in the encoder speech processing subsystem, as described in paragraph 5.3.2.1.3 and shown on Figure 5-49.

9. Three AND gates (A1, A2, and A3) are used to perform logic functions. Each provides an output signal only when all of its input signals are present simultaneously. The circuit is similar to that described in paragraph 5.3.1.7.6.8 and shown schematically on Figure 5-36.

10. An OR gate (O1) is used to perform a logic function. An output signal is produced in response to either of two input signals or to both such signals. The circuit is similar to that described in paragraph 5.3.1.7.6.9 and shown schematically on Figure 5-37.

11. Four Inhibit AND gates (AI1, AI2, AI3, and AI4) are used. In each case the gate allows a signal received at its signal input terminal to be transmitted from the signal output terminal except when another signal, the inhibiting signal, is simultaneously present at the gate's inhibit input terminal. The circuit used is similar to that described in paragraph 5.3.1.7.6.10 and shown schematically on Figure 5-38.

5.4.2.2.4 Logic Operation

The decoder pulse-to-speech demodulation subsystem, shown in logic diagram form on Figure 5-73, operates as follows.

The clock pulse generator produces a series, or train, of locally generated clock pulses in response to sync pulses supplied by the decoder sync subsystem. The sync pulses assure that the locally generated clock pulses are synchronized in both phase and frequency with the clock pulses produced by the encoder sync subsystem to serve as modulation reference pulses.

The locally generated clock pulses each trigger a monostable multivibrator, MS1, to produce windows, or gating intervals, during which speech pulses received from the spacecraft via the tracking radar set's video detector are allowed to enter the decoder pulse-to-speech demodulation subsystem. The duration of each window corresponds to the ON period of the monostable multivibrator.

Arrival of a speech pulse in the demodulation subsystem during a window causes two capacitors to be alternately charged and subsequently, and again alternately, discharged. At the end of the window period the charge circuit associated with the first capacitor to have been charged is switched OFF and the magnitude of the charge placed on the capacitor is determined. Concurrently, the subsystem prepares (through suitable logic switching operations) to allow the second capacitor to be charged in response to the next speech pulse to occur during a window.

The logic arrangement used permits the two capacitors (C1 and C2, as shown on Figure 5-73) to be charged and discharged alternately. As the second capacitor is being charged, the magnitude of the charge placed on the first capacitor is being determined. As soon as the second capacitor is charged and while the magnitude of the voltage placed on it is being determined, the first capacitor is discharged in preparation for a repetition of the charge, charge determination, discharge cycle.

The switching action necessary to charge first one and then the other capacitor is provided by a commutating flip-flop (FF1). This flip-flop is set to a ONE state in response to a signal produced by an AND gate (A1) when a speech pulse is received during the ON period of the monostable multivibrator (MS1). The flip-flop is automatically reset to a ZERO state at the end of each ON period through action of a trailing edge pulse generator (TEPG1).

The voltages stored alternately on the capacitors are directly proportional to the time modulation interval of the speech pulses: the later the speech pulse occurs during the window, or gating interval, the lower the charge placed on the capacitor. Conversely, the earlier the speech pulse occurs during the window, the greater the charge placed on the capacitor.

These conditions are just the opposite from those existing in the encoder during the process of forming the pulse position modulated speech pulses.

There, the later a speech pulse occurs during the gating interval, the greater the voltage, while the earlier it occurs, the lower the voltage. Accordingly, a phase inverter is incorporated in the demodulation subsystem to invert the decoder pulse-to-speech demodulation subsystem's output signal. This signal is a synchronous rectangular audio signal whose waveform is a rectangular facsimile of the waveform of the audio signal applied to the encoder system.

A timing diagram which indicates the relationship between various encoder and decoder system operational events is shown on Figure 5-42.

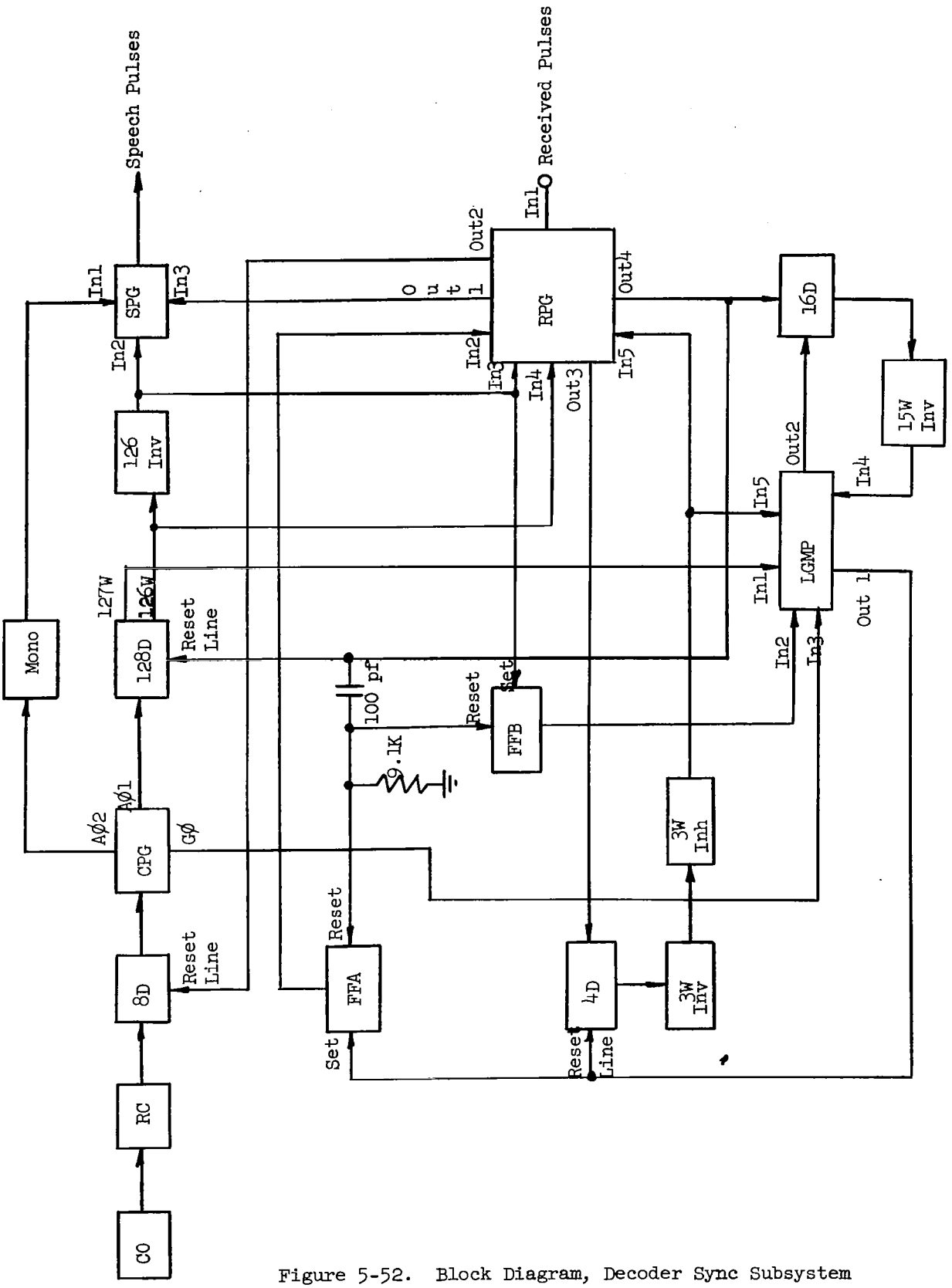


Figure 5-52. Block Diagram, Decoder Sync Subsystem

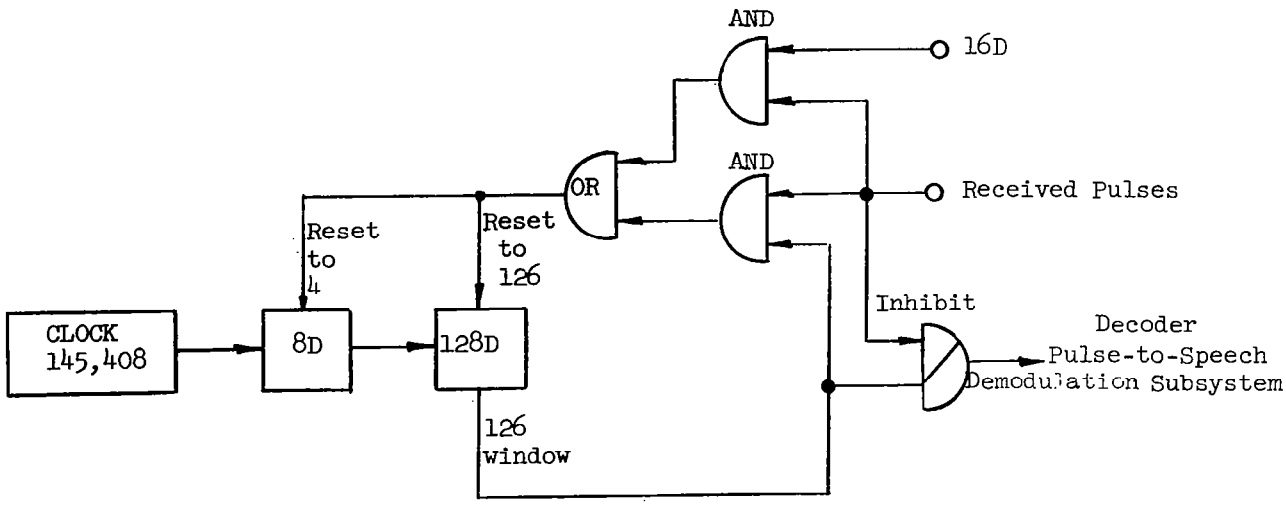


Figure 5-53. Block Diagram, Decoder Sync Subsystem Sync Pulse Gating Components

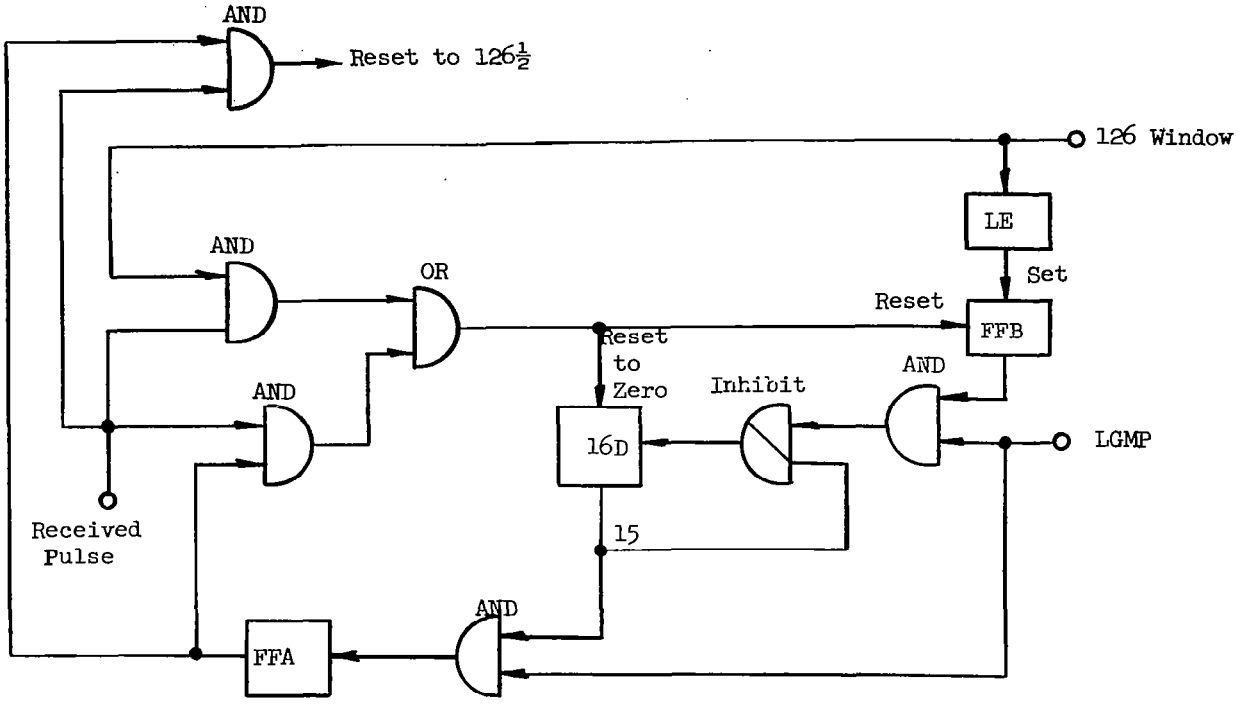


Figure 5-54. Block Diagram, Decoder Sync Subsystem Acquisition Mode Components

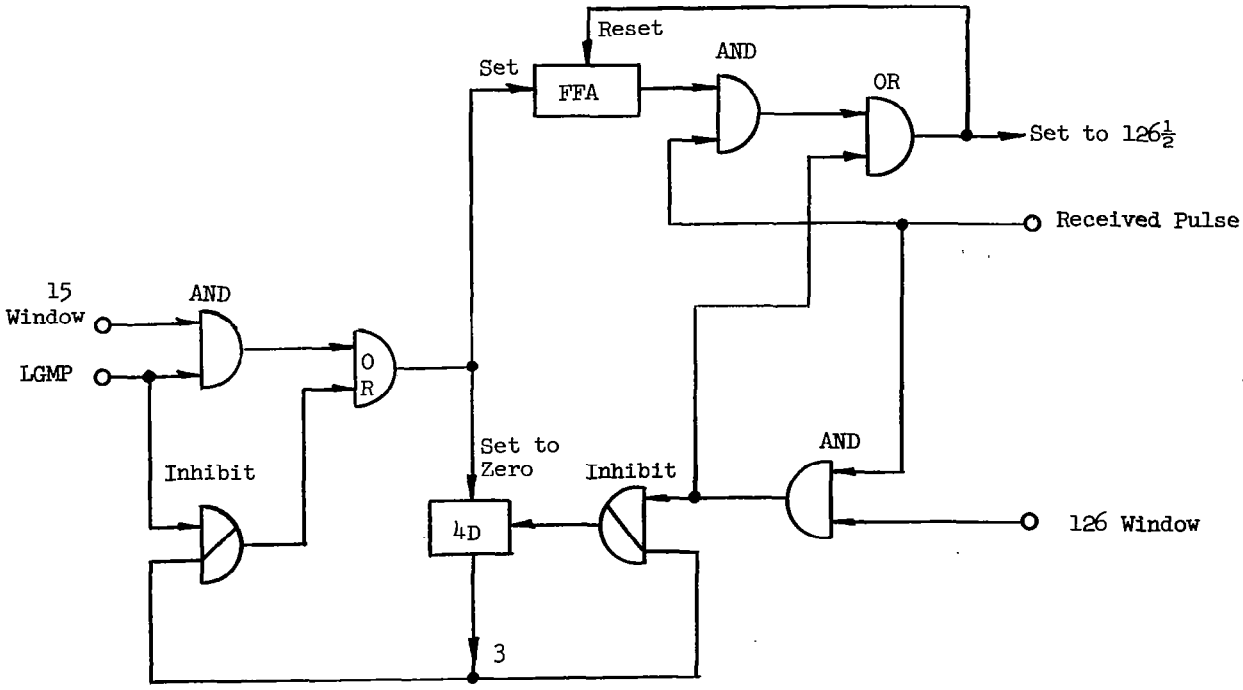


Figure 5-55. Block Diagram, Decoder Sync Subsystem
In Sync Mode Components

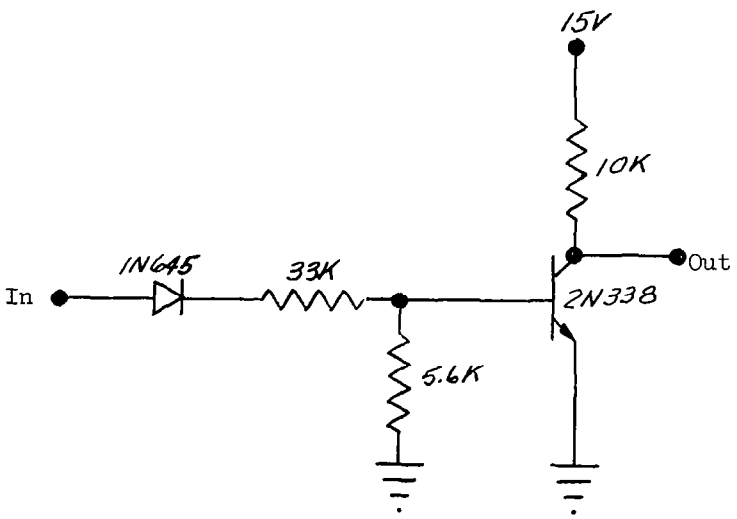


Figure 5-56. Schematic Diagram, 126-Window Inverter

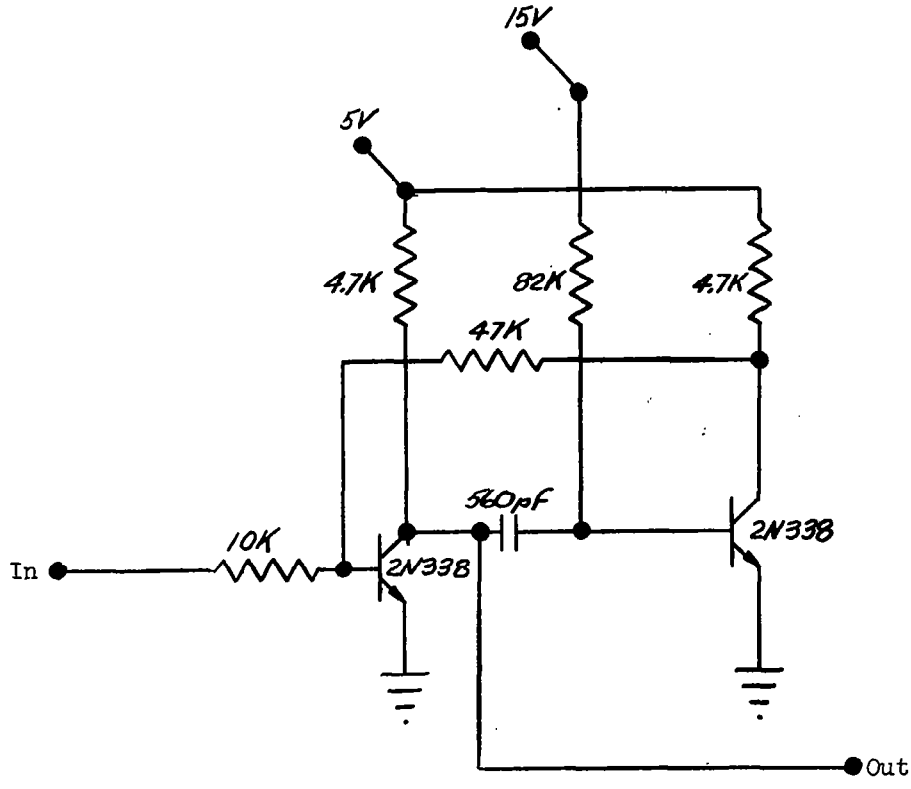


Figure 5-57. Schematic Diagram, Speech Monostable Multivibrator

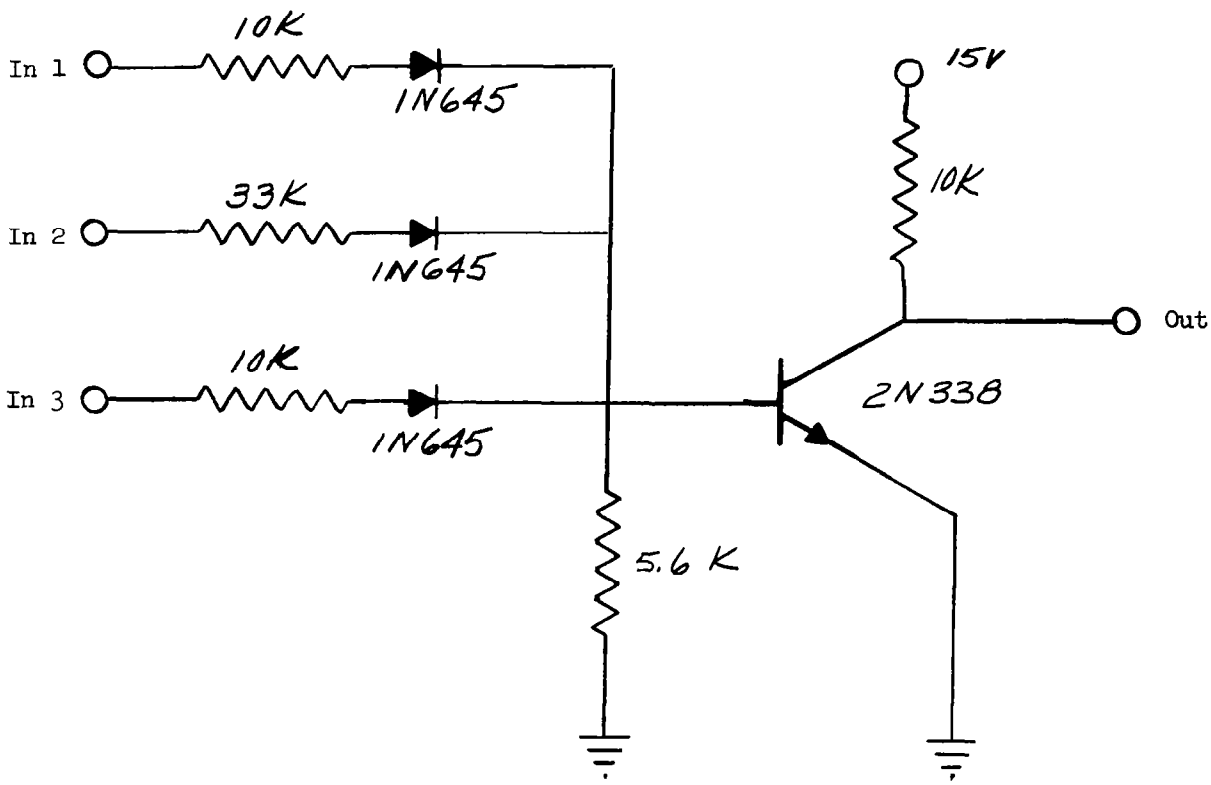


Figure 5-58. Schematic Diagram, Speech Pulse Gate

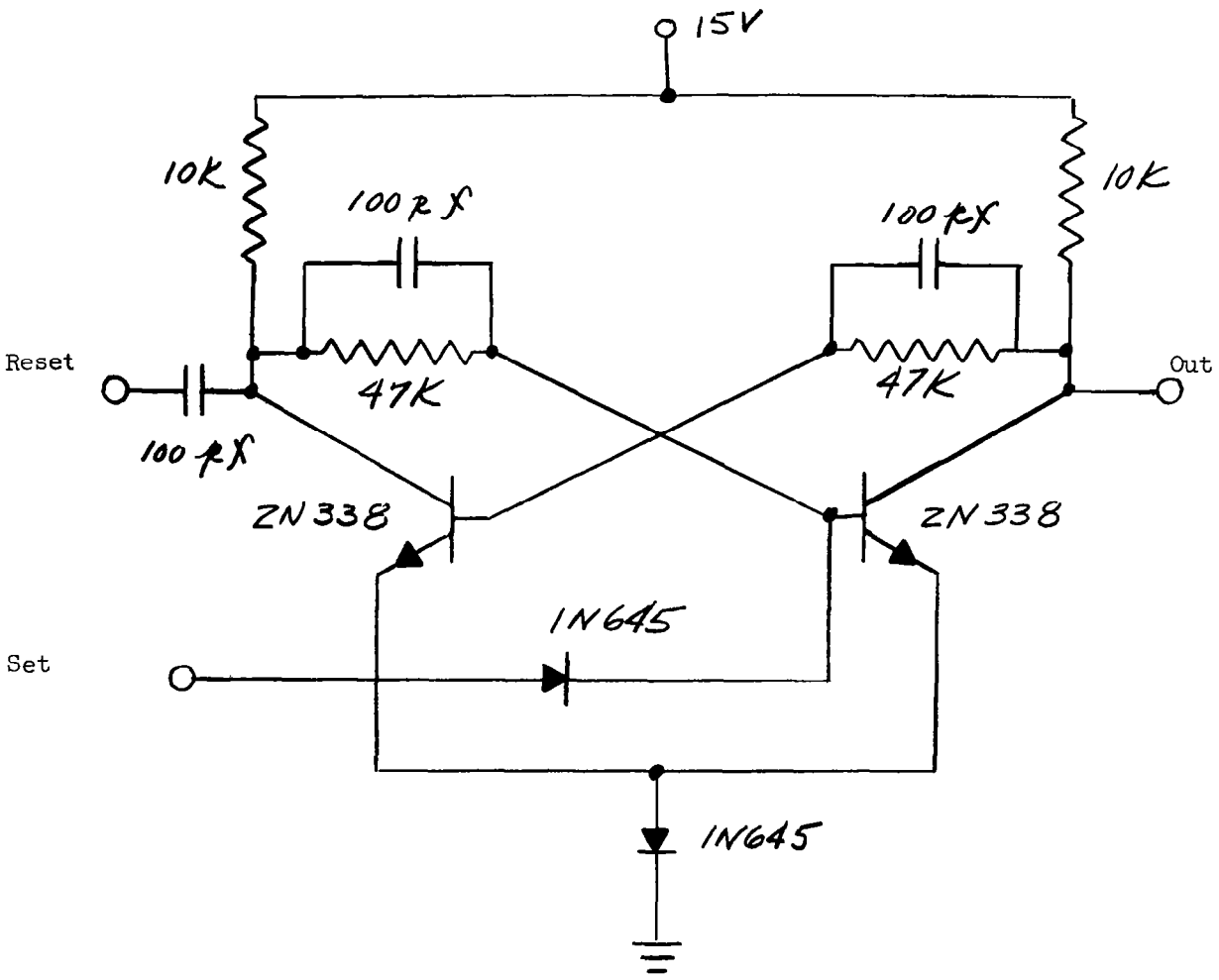


Figure 5-59. Schematic Diagram, Flip-Flop A

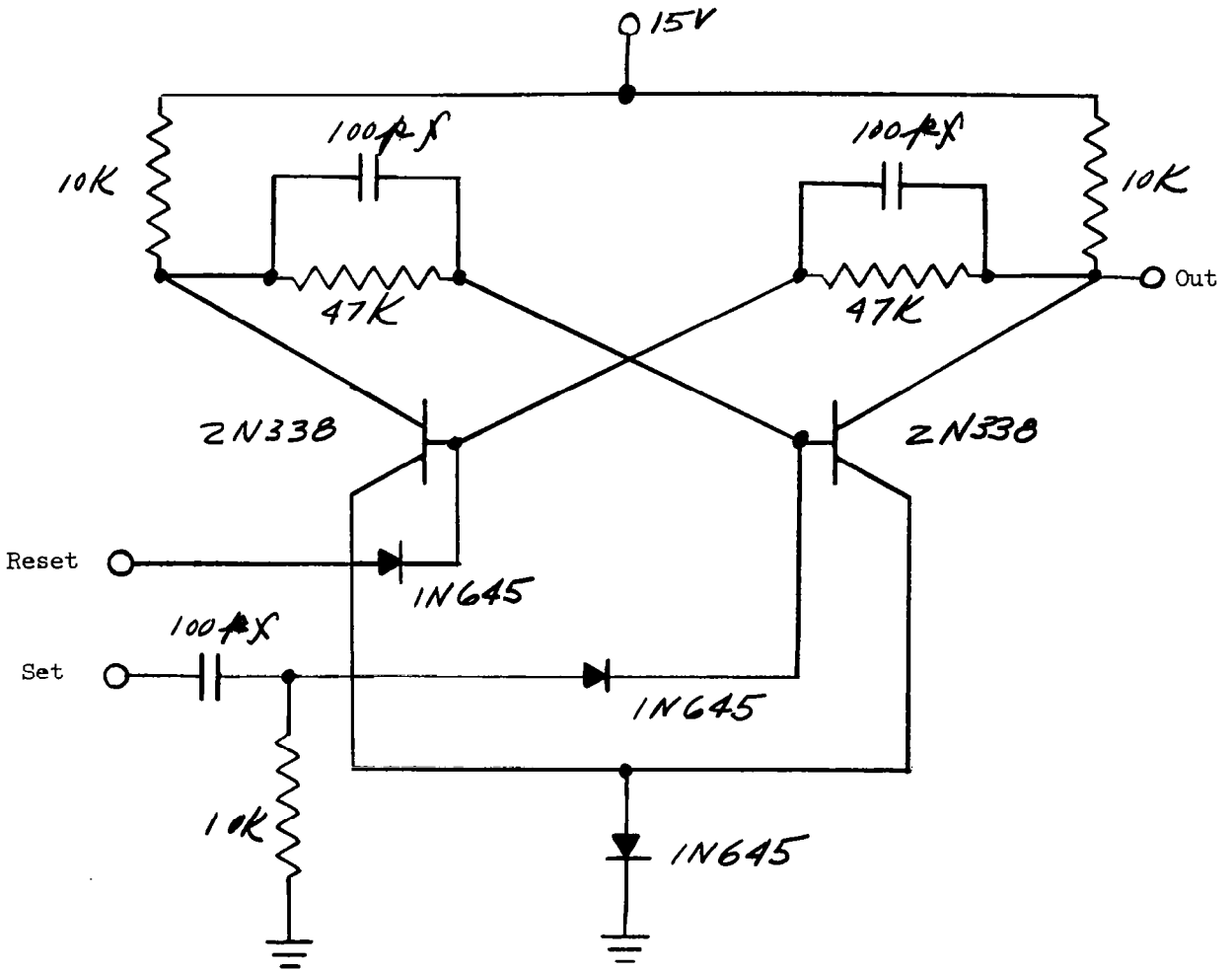


Figure 5-60. Schematic Diagram, Flip-Flop B

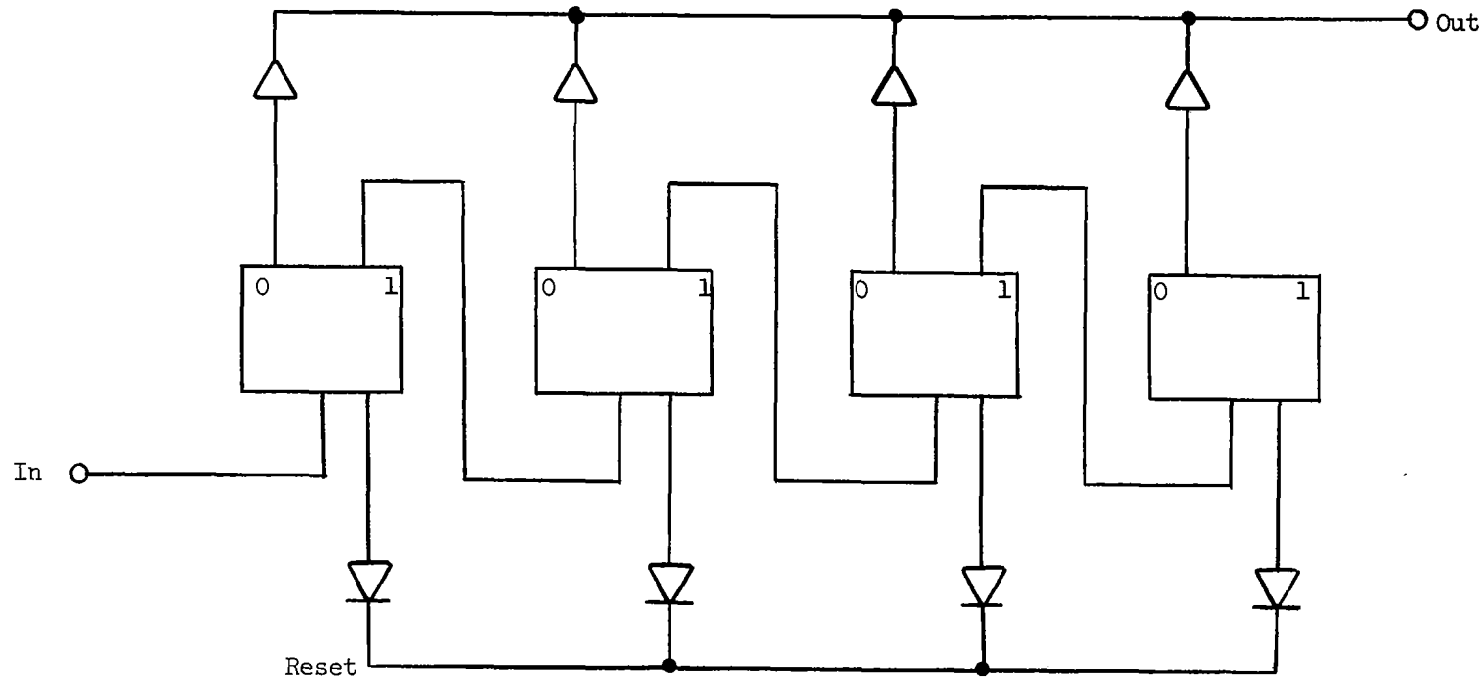


Figure 5-61. Logic Arrangement, Divide-by-16 Divider

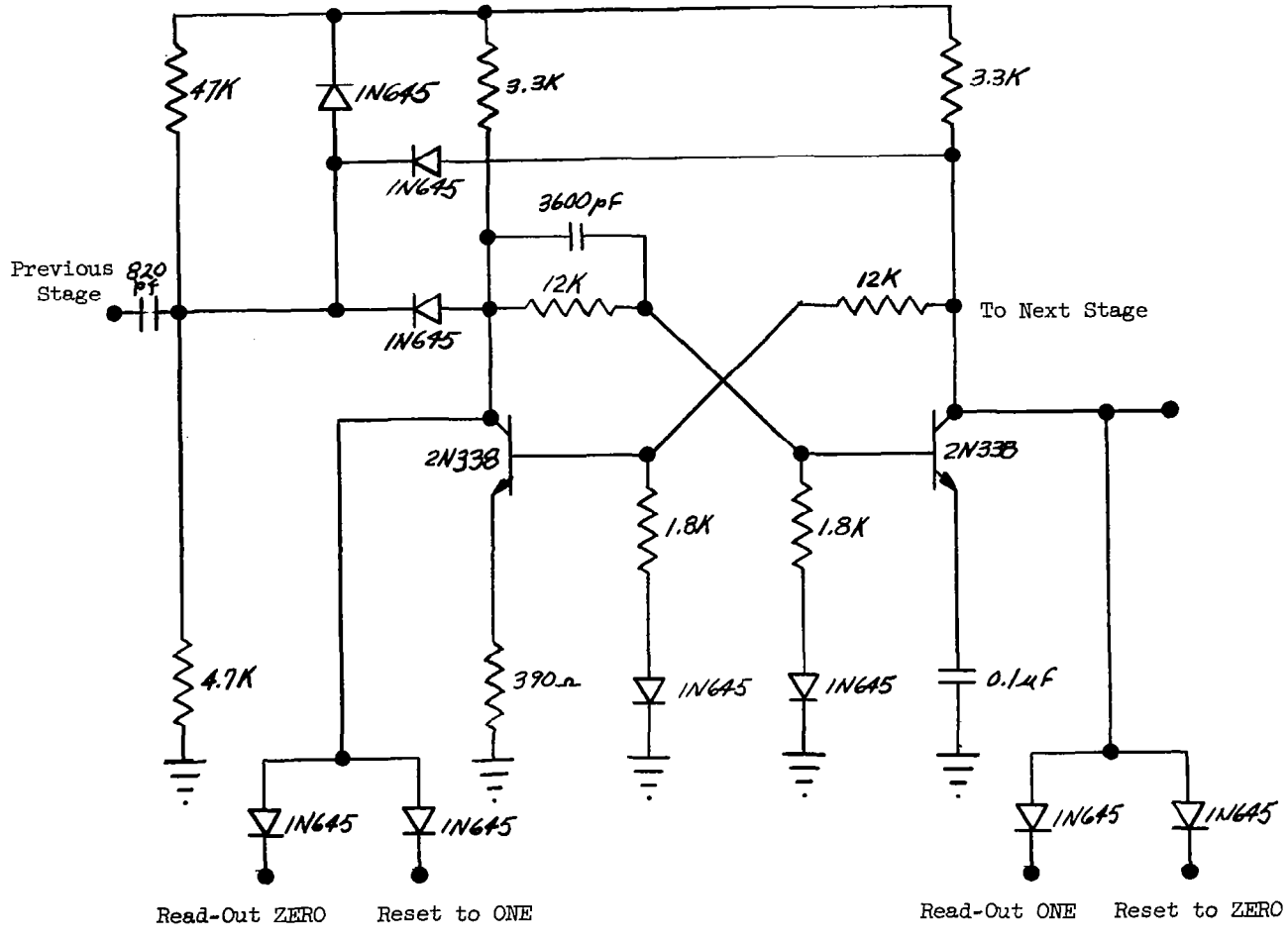


Figure 5-62. Schematic Diagram, Typical Stage of Divide-by-Four and Divide-by-16 Dividers

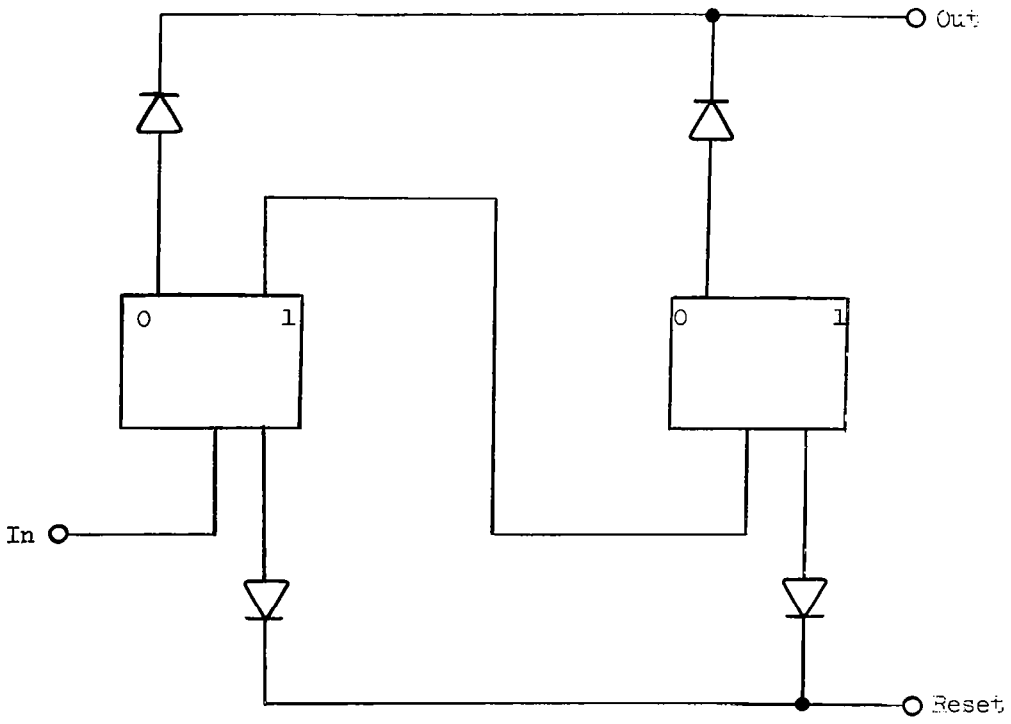


Figure 5-63. Logic Arrangement, Divide-by-Four Divider

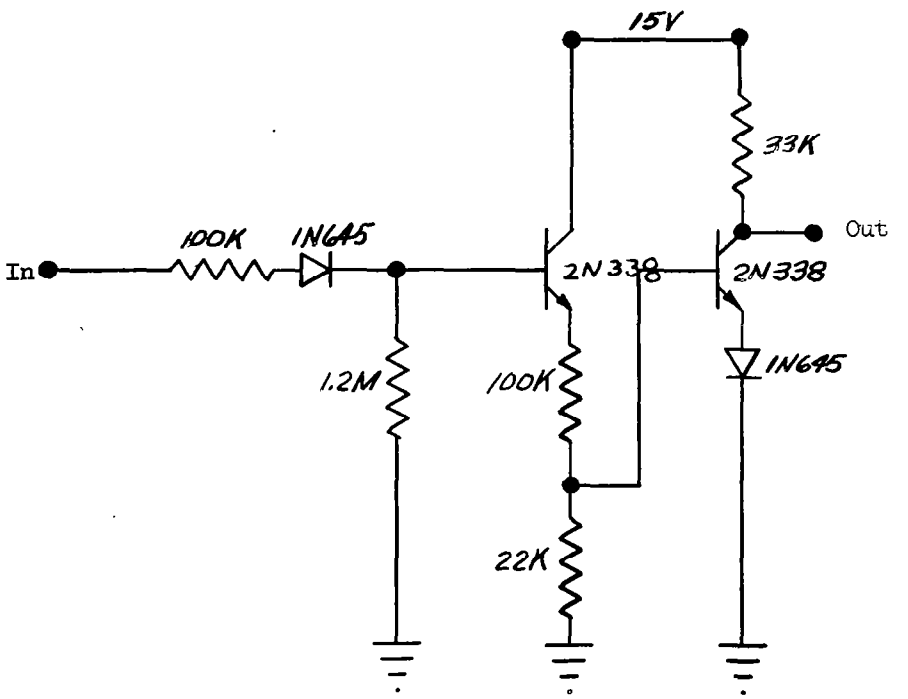


Figure 5-64. Schematic Diagram, 15-Window and 3-Window Inverters

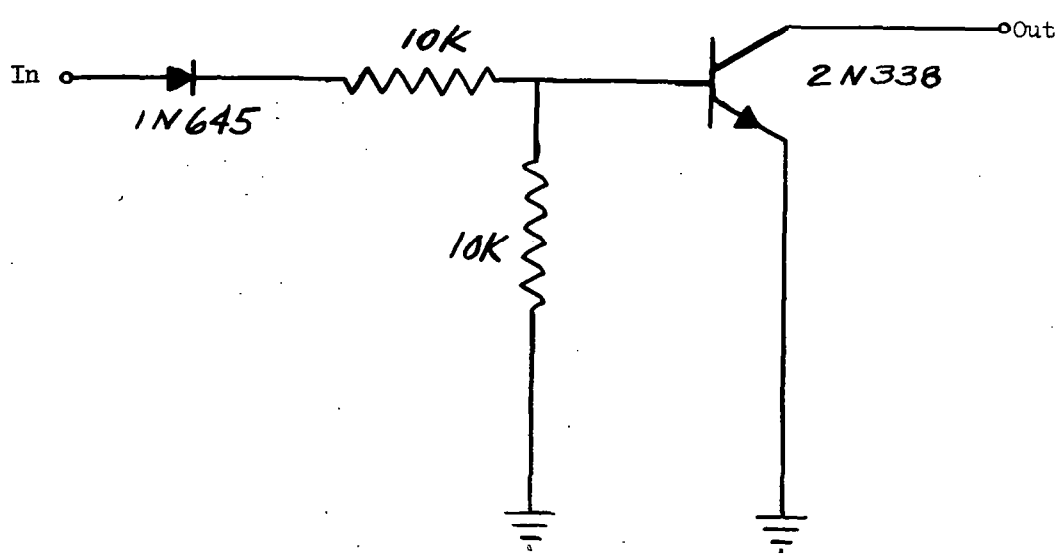


Figure 5-65. Schematic Diagram, 3-Window Inhibit Gate

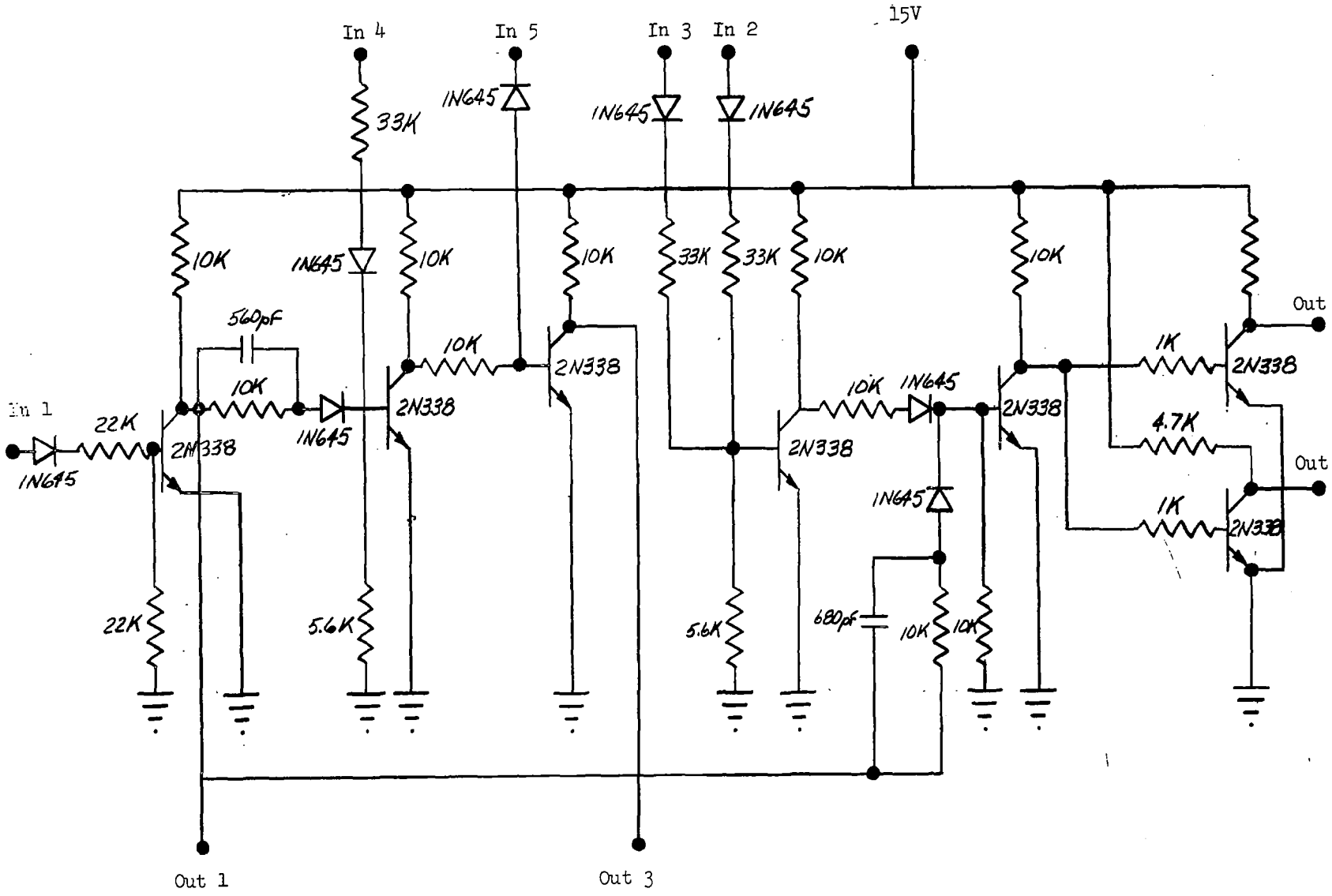


Figure 5-66. Schematic Diagram, Received Pulse Gate

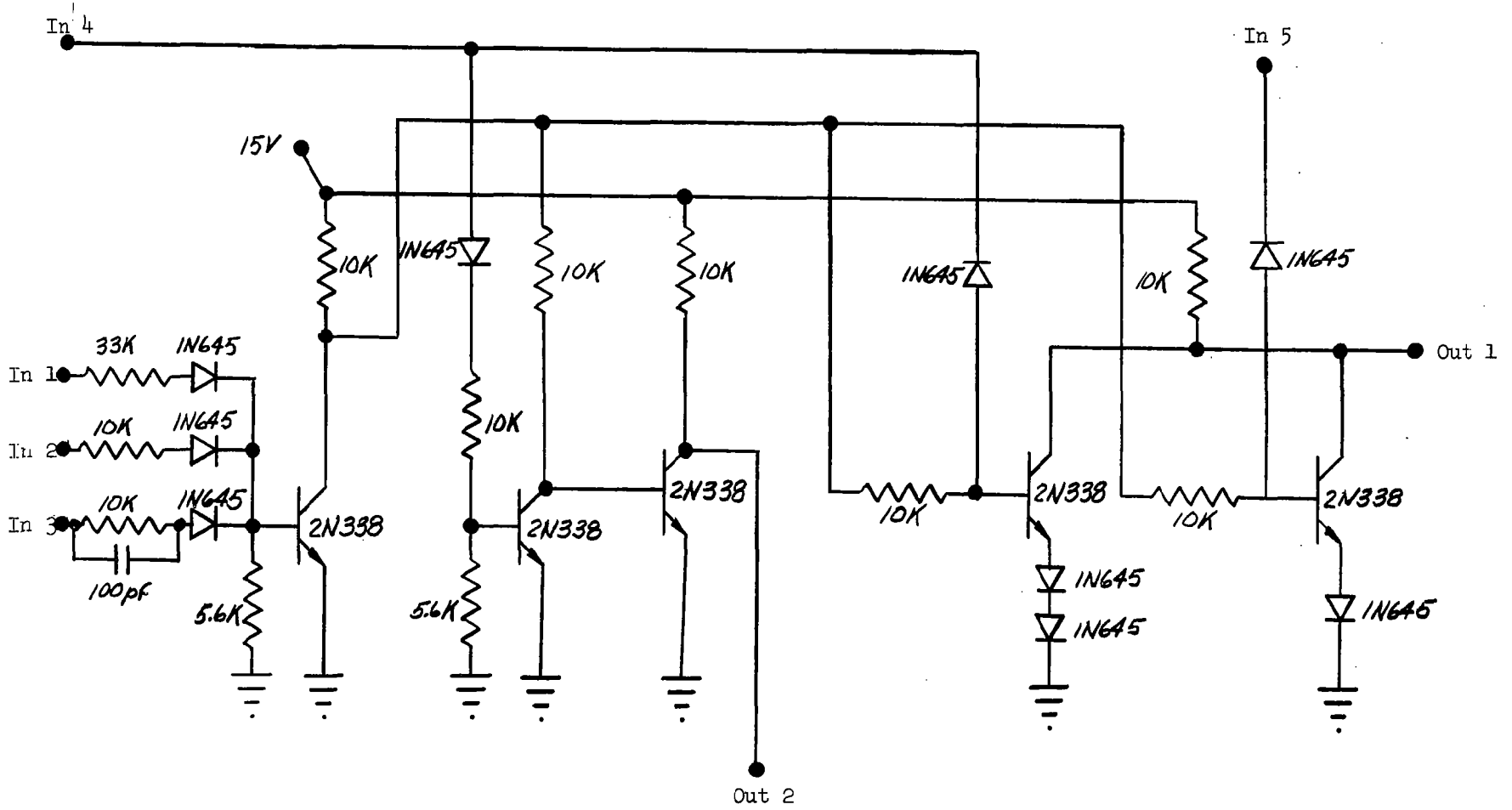


Figure 5-67. Schematic Diagram, Locally Generated Miss Pulse Gate

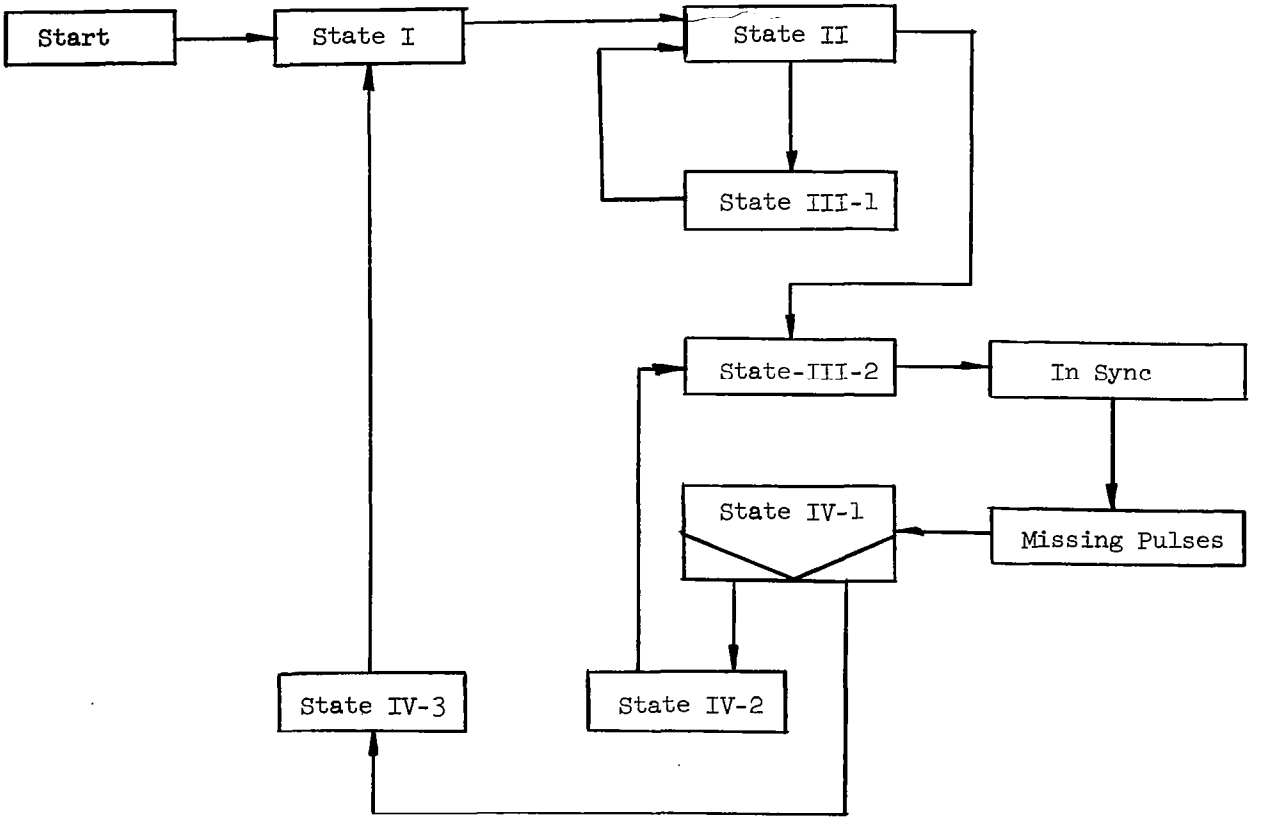
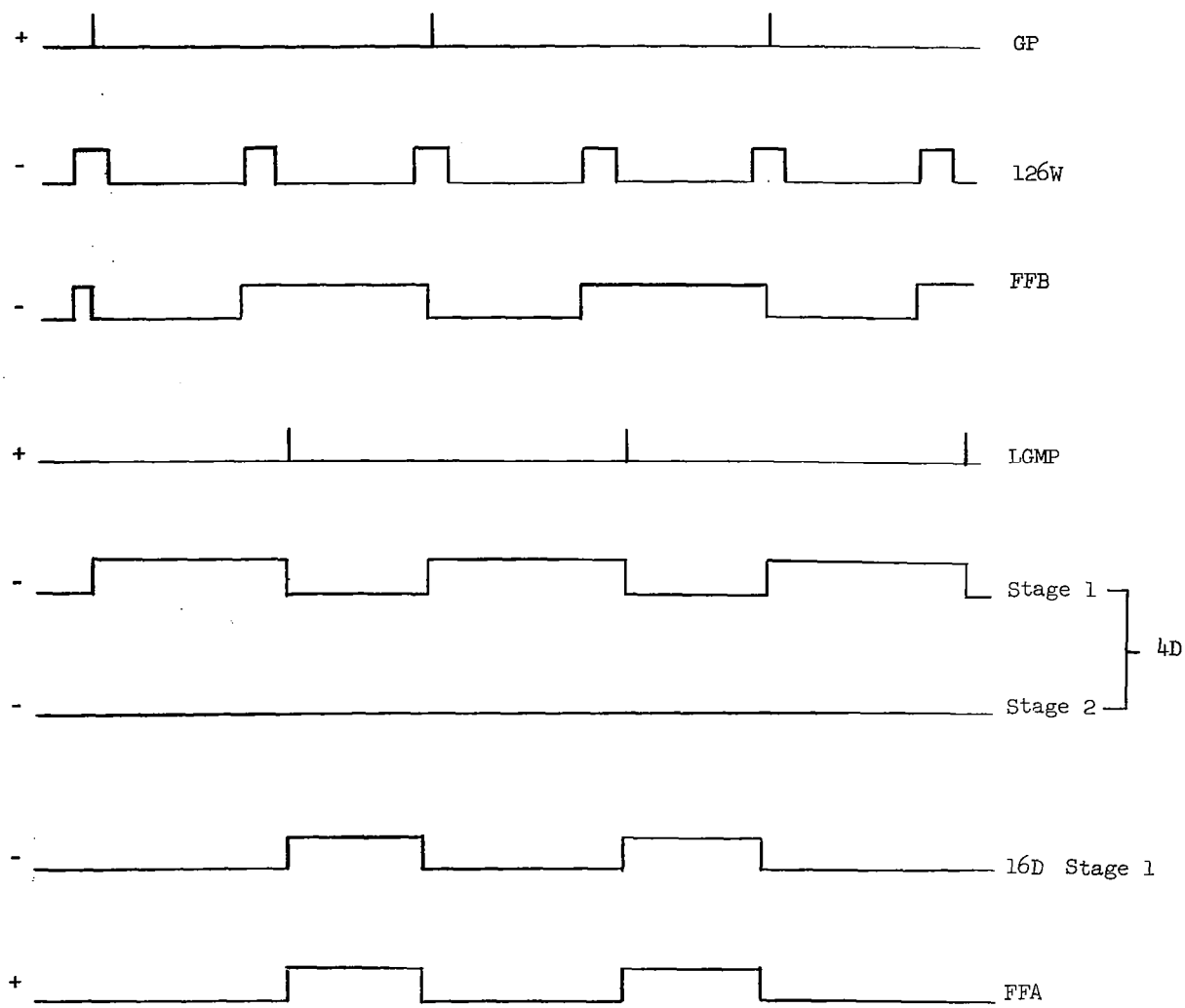
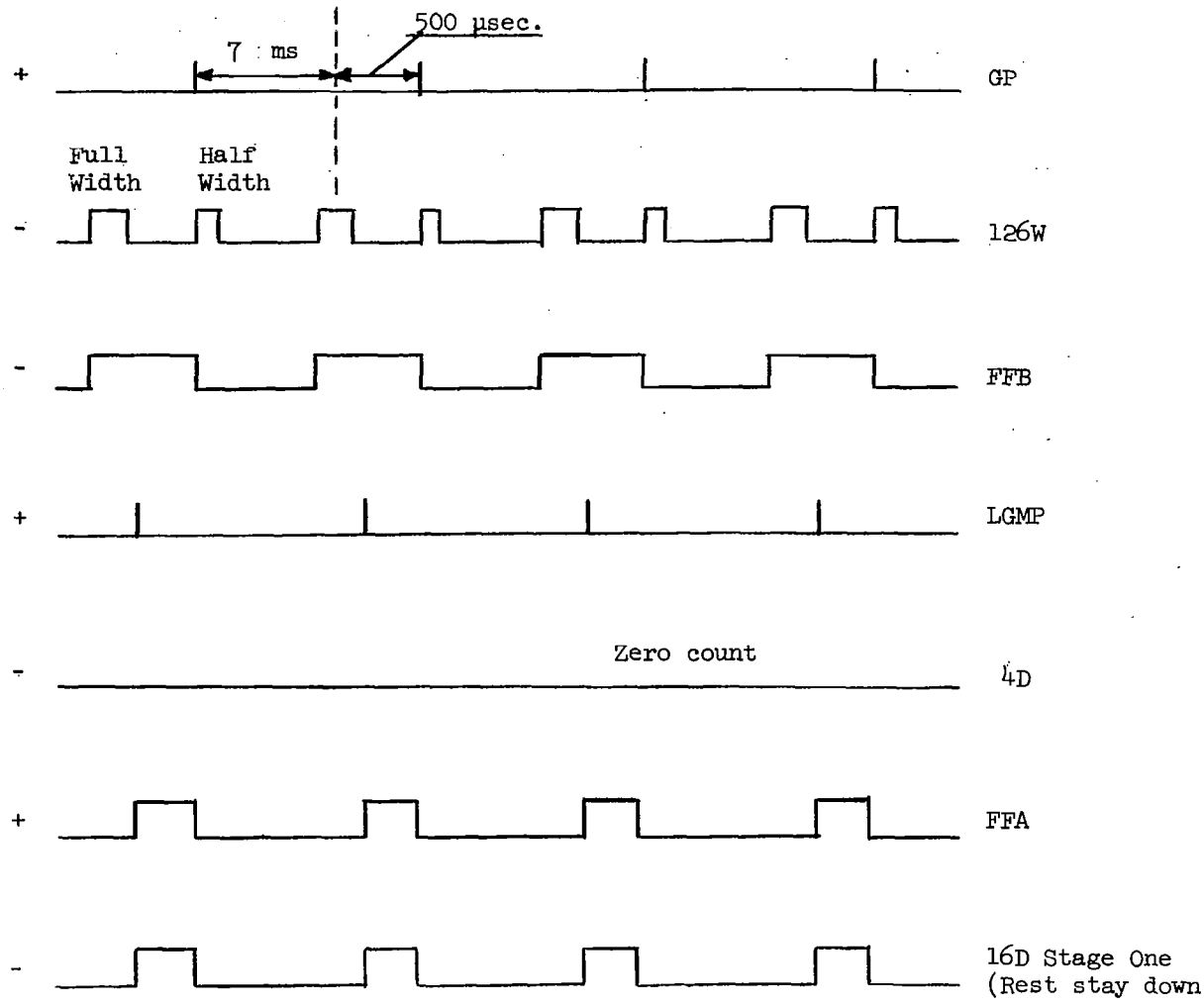


Figure 5-68. Flow Diagram, Decoder Sync Subsystem Logic States



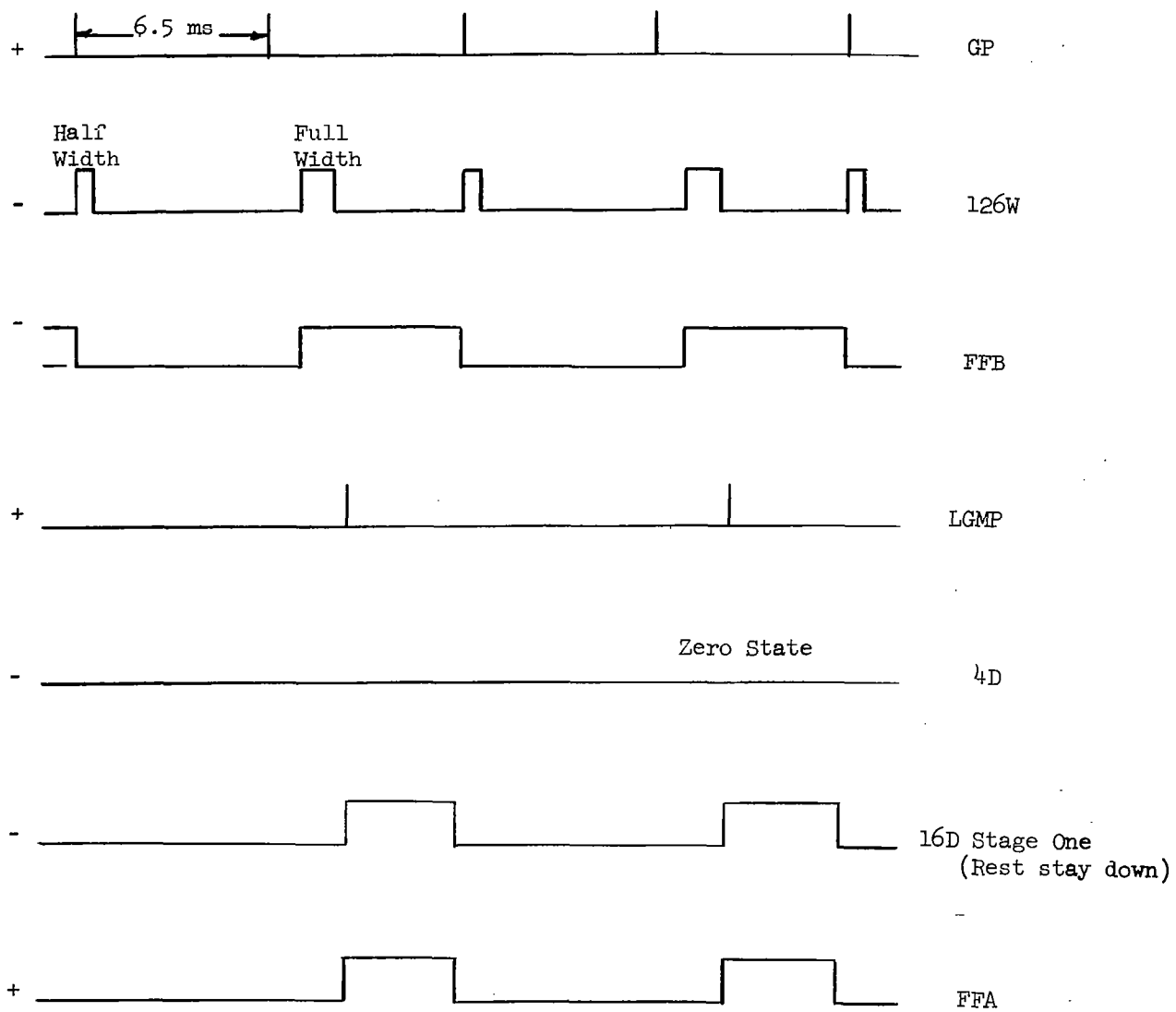
(a) 4D counts 0 to 1 to 0
(b) 16D counts 0 to 1 to 0
(c) FFA set & reset
(d) FFB set by 126W & reset

Figure 5-69. Decoder Sync Subsystem Timing Diagram, Missing Every Other Pulse



NOTE: Ground pulse arrives 500 µsec. late.

Figure 5-70. Decoder Sync Subsystem Timing Diagram, Ground Pulse Frequency Low



NOTE: Ground pulse arrives 500 μsec. early.

Figure 5-71. Decoder Sync Subsystem Timing Diagram, Ground Pulse Frequency High

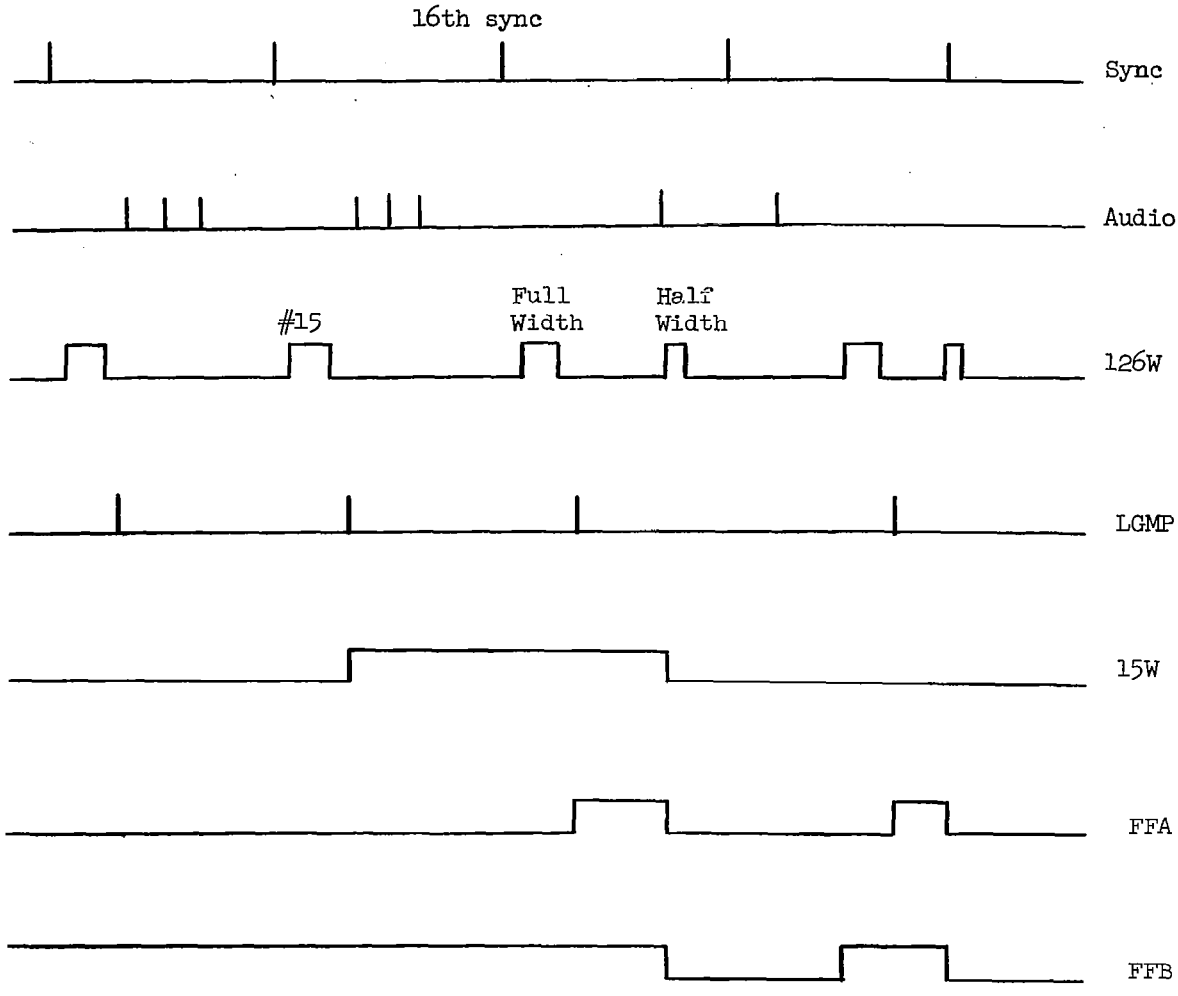


Figure 5-72. Decoder Sync Subsystem Timing Diagram,
Sync Pulses and Random Audio Out of Sync

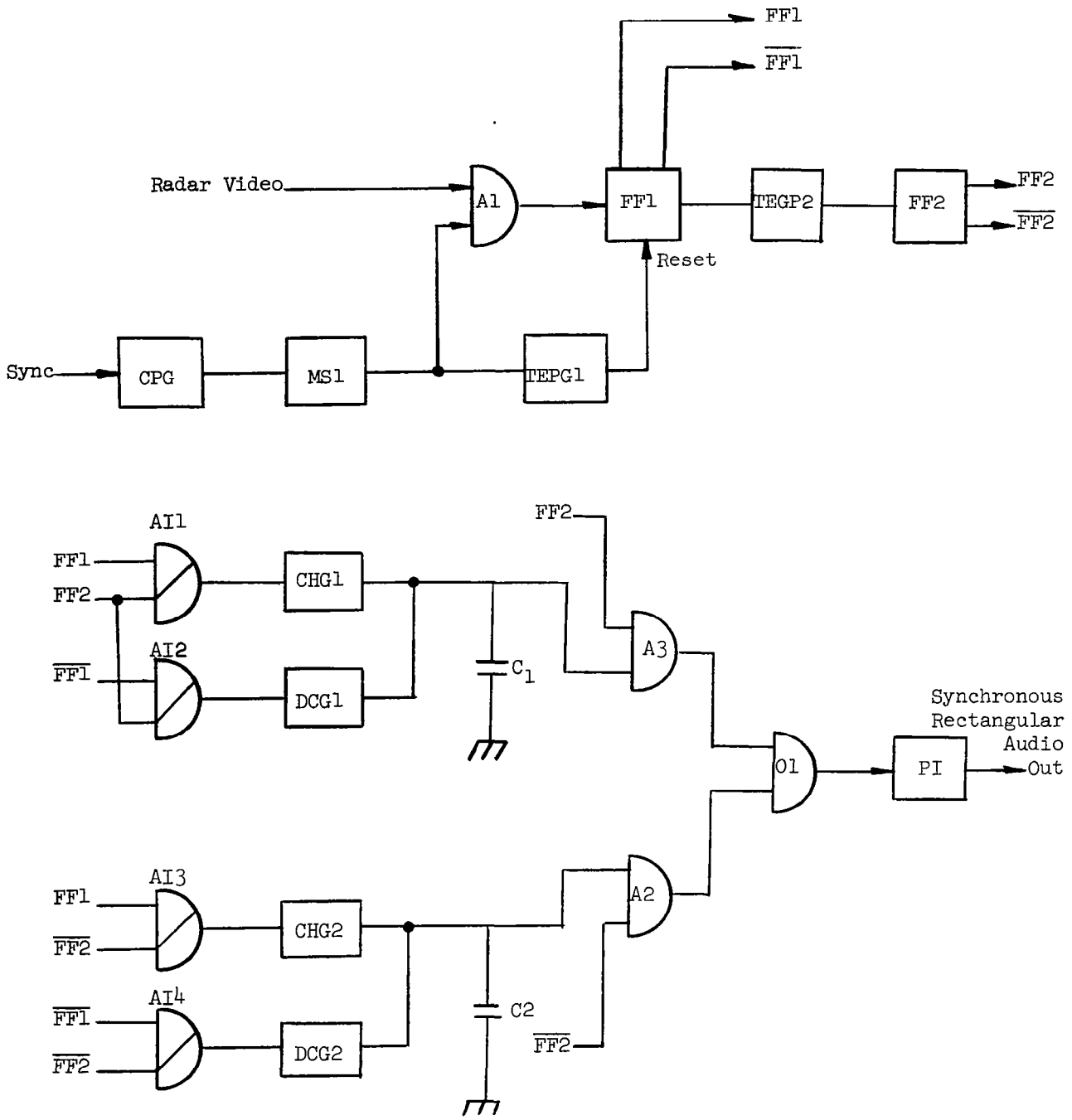


Figure 5-73. Logic Diagram, Decoder Pulse-to-Speech Demodulation System

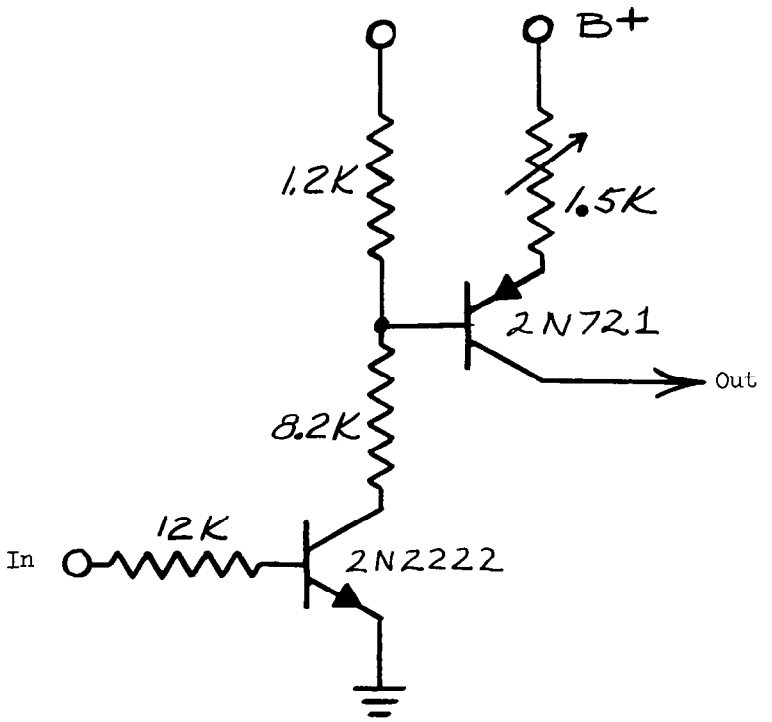


Figure 5-74. Schematic Diagram, Charge Circuit

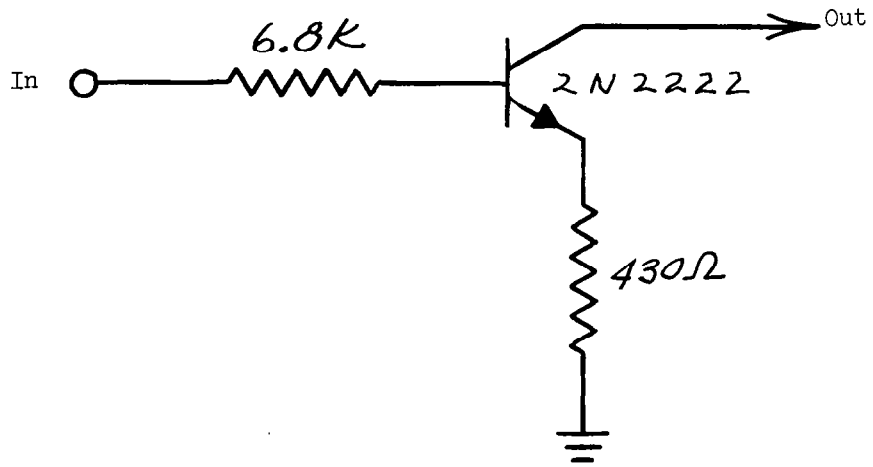


Figure 5-75. Schematic Diagram, Discharge Circuit

5.5 ASTROVOICE/RADAR TRACKING EQUIPMENT INTERFACE INVESTIGATION AND ANALYSIS

The interface between the Astrovoice II system and the radar tracking equipment was investigated and analyzed as directed in Task II of Contract No. NASw-586. Results of these investigations and analyses are presented here as follows:

Paragraph 5.5.1 (and its subparagraphs)	The interface between the Astrovoice II system and various ground-based tracking radar equipment.
Paragraph 5.5.2 (and its subparagraphs)	The interface between the Astrovoice II system and various tracking radar beacons.

5.5.1 Astrovoice Radar Tracking Equipment Interface

5.5.1.1 Pulse Rates

Effective this year, 1964, pulse rates for all radar tracking equipment to be used on an inter-range basis will be standardized. The standard pulse rates, as defined by the Inter-Range Instrumentation Group (IRIG) are:

80 pulses per second (pps)
160 pulses per second (pps)
320 pulses per second (pps)
640 pulses per second (pps)

These standard pulse rates will be employed on the following-listed ranges:

Air Force Flight Test Center (AFFTC)
Air Proving Ground Center (APGC)
Atlantic Missile Range (AMR)
Naval Ordnance Test Station (NOTS)
Pacific Missile Range (PMR)
White Sands Missile Range (WSMR)

Once the pulse rate standards become effective, any radar tracking equipment to be used on an inter-range basis will be required to operate at one of the standard pulse rates.

The interface discussion presented in this portion of the report will, accordingly, be based generally upon the assumption that these standards will be in effect. Although the previous descriptions of encoder and decoder system operation (paragraphs 5.3 and 5.4 and their respective subparagraphs) were written on the basis that the Astrovoice II system is being operated in conjunction with the AN/FPS-16 radar tracking equipment which has a presently standard pulse rate of 142 pps, modification of the Astrovoice II system to

operate with radar equipment transmitting at one of the new standard rates (or any integral multiple of one of these rates) is essentially simple. As noted in paragraphs 5.3 and 5.4, modification generally would require only selection of a suitable clock rate and, possibly, use of different dividers.

In modifying the Astrovoice II encoder system to enable it to operate with radar tracking equipment using the new standard pulse rates, a basic clock rate compatible with the most commonly used pulse rate would be selected. Suitable provision would also be made for inhibiting transmission of speech pulses during the intervals at which ground pulses at that rate are expected to arrive at the beacon. The inhibit logic and circuits, as noted in paragraph 5.3, are used to prevent spurious return signals and to prevent ground pulse lock-out, sometimes described as radar count down. If such logic and circuits were not provided, lock-out of up to 20% of the ground pulses could occur.

Modification of the Astrovoice II system to enable it to operate in conjunction with radar equipment employing the lowest standard pulse rate (80 pps) would require that the dividers in the encoder sync subsystem (as well as the delay shift register in the encoder sync system designed to protect ground pulses coming from several tracking radar equipments) provide the proper inhibit intervals for the 80 pps rate and for any integral multiple of that rate. Assuming that the system had been so modified, the maximum lock-out which could occur if the Astrovoice II system were then operated in conjunction with radar equipment transmitting at any other rate would be 20%.

The effect of a change in pulse rates necessary to enable tracking in an interference zone is described in paragraph 5.5.1.5.

5.5.1.2 Probable Ground or Ship Based Radar Tracking Equipment

Investigations indicated that the Astrovoice II system would most probably be used in conjunction with one or more of the following-listed ground or ship based radar receiving and tracking equipments:

Type	Base	Notes
AN/FPQ-4	Ground and Ship	This radar set was the predecessor of the AN/FPS-16 radar set. It is used as either ground-based or ship-based equipment. In ship-based use it is installed on the Down-range Anti-missile Measurement Program (DAMP) ship.

Type	Base	Notes
AN/FPS-16	Ground and Ship	Used as either ground-based or ship-based equipment. In ship-based use it is installed on the USS Twin Falls Victory. It is also used, with suitable modifications, as a mobile ground-based radar set, the AN/MPS-25.
AN/MPS-25	Ground	This is a mobile version of the AN/FPS-16 radar set.
AN/FPQ-6	Ground	Used as a fixed ground-based radar set. With suitable modifications (as AN/TPQ-18), it is also used as a mobile ground-based radar set.
AN/TPQ-18	Ground	This is a mobile version of the AN/FPQ-6 radar set.
Sperry	Ship	Used in Advanced Range Instrumentation Ship (ARIS) installations.

The type FPQ-4 radar set is capable of tracking at ranges up to 500 nautical miles (nm). It has provisions for semi-automatic target acquisition. It presently has no provisions for either pulse code group transmission or automatic phasing.

The type FPS-16 radar set has been modified to enable it to track at ranges up to 5,000 nm. It has provisions for pulse code group transmission, automatic target acquisition*, and automatic phasing.

The type FPQ-6 radar set is capable of tracking at ranges up to 32,000 nm. It has provisions for automatic target acquisition and automatic phasing. Although this type of radar set is not presently capable of pulse code group transmission, this capability is scheduled to be incorporated.

The Sperry radar equipment used on the ARIS is capable of tracking at ranges up to 32,000 nm. These sets have provisions for pulse code group transmission and for automatic target acquisition. They are scheduled to be equipped with automatic phasing equipment during calendar year 1964.

5.5.1.3 External Connections--Astrovoice to Radar Tracking Equipment

Investigation into the interface between the Astrovoice II system and ground-based type FPQ-4, FPQ-6, FPS-16, TPQ-18 and MPS-25 radar equipment, particularly

* Some FPS-166 radar sets are equipped, however, with semi-automatic instead of automatic acquisition systems.

in the area of external connections, indicated that the Astrovoice II system is required to be compatible with the following-listed radar equipment characteristics.

Non-tracking video detector output (standard pulses)	0.75 to 2 volts, 75 to 93 ohms impedance.
Pre-pulse output preceding the 'main bang' output	Same as non-tracking video output (0.75 to 2.0 volts, 75 to 93 ohms impedance).
Video pulse	Includes both skin and beacon returns.

When using the Astrovoice II system with any of these types of radar equipment for receipt of speech pulses, the skin local oscillator of the radar equipment must be turned off to eliminate skin frequency returns. Speech pulses from the spacecraft cannot be properly demodulated in the decoder system if the skin local oscillator is ON (a condition which provides skin frequency returns).

A similar investigation into the interface between the Astrovoice II system and the Sperry radar equipment used on ARIS indicated that the Astrovoice II system is required to be compatible with the following-listed radar equipment characteristics.

Non-tracking video output	50 volts
Video output pulse duration	0.6 usec
Pre-pulse output preceding the 'main bang' output	Same as non-tracking video output (50 volts)
Video pulse	Beacon return only.

Atlantic Missile Range personnel have suggested that a simple cathode-follower type isolation circuit be used between the Astrovoice II system and the video detector output of the Sperry radar equipment.

5.5.1.4 Operational Considerations.

Consideration of various aspects of operation of the radar equipment in conjunction with the Astrovoice II system indicated that no difficulty would be experienced during operation of the radar equipment in either the semi-automatic acquisition mode or the manual phasing mode. Operation of the radar equipment in the automatic acquisition mode or the automatic phasing mode does, however, present certain problems, none of which appear insoluble. Descriptions of the various modes of operation, of the problems presented when operating in either of the two automatic modes (acquisition or phasing), and of the possible solutions to these problems follow.

5.5.1.4.1 Acquisition

The semi-automatic acquisition mode can be used if the azimuth and elevation coordinates of the target are known. In this mode of operation, the operator acquires the target by positioning the range gate by suitable manually-operated controls. The presence of speech pulses in the beacon return signal train will present no difficulty when operating in this mode since the speech pulses are random in time in respect to the tracking return pulses from the beacon. Once the target is acquired, the radar set will track the target in the automatic mode.

The effect of incorporation of fully automatic acquisition mode capabilities in radar equipments has been studied. Many radar sets have recently been modified to incorporate this capability. Others are scheduled to be similarly modified. Radar sets capable of automatic target acquisition transmit either a two-pulse pattern or a phase-jumped alternating pattern, according to the particular type of radar set involved. The FPQ-6 and the FPS-16 radar sets use a two-pulse pattern: the Sperry sets use a phase-jumped alternating pattern. In either case, knowledge of the actual or projected coordinates of the target is used as much as possible to facilitate automatic acquisition. Digital detection circuits are included in the radar equipment to enable identification of the characteristic return pattern (two pulse or phase-jumped alternating) as the radar pulses search a given volume of space. Presence of speech pulses in the beacon return signal train can confuse the automatic acquisition system in its attempts to lock onto the target since the speech pulses will resemble return pulses (although, of course, spurious) insofar as the automatic acquisition system is concerned. Although the presence of speech pulses in the transmission from the beacon could be of material assistance to a suitably designed radar set in determining the azimuth and elevation coordinates of the target due to the highly directional nature of the radar tracking antennas, present automatic acquisition systems are not designed to make advantageous use of this assistance.

After analyzing these aspects of radar equipment operation and discussing them with Atlantic Missile Range (AMR) personnel, it was concluded that:

1. Use of semi-automatic acquisition techniques is suitable either when the target coordinates are previously and relatively accurately known or when rapid acquisition is not essential.

2. The ability to acquire the target automatically is essential when the coordinates are not known with sufficient accuracy or when rapid acquisition is imperative.

Accordingly, a method of inhibiting speech pulses should be provided to avoid confusing the radar equipment when it is operating in the automatic acquisition mode.

One feasible method of inhibiting speech pulses requires that the radar equipment be capable of transmitting coded pulse groups. This capability already exists in most types of radar sets with which the Astrovoice II system is

likely to be used. In this method, if a beacon normally responsive to a two-pulse code is interrogated by a three-pulse code in which the first two pulses are identical to those in the two-pulse code, the beacon transmits its normal reply. The third pulse is detected by the Astrovoice encoder system and identified as an inhibit signal. The encoder would then inhibit transmission of speech pulses during the time the three-pulse code group was being transmitted to the beacon by any radar set. In addition, speech pulse transmission would also be inhibited for a suitable interval following transmission of such a pulse group. Discussions with Radio Corporation of America (RCA) personnel indicated that modifications to enable transmission of appropriate pulse groups could be accomplished with relative ease.

5.5.1.4.2 Phasing

When operating in the manual phasing mode, the relative phasing of pulse trains from various radars used in tracking is controlled manually by a control radar operator, or controller. If the pulses from one radar set begin to drift too close to pulses from another radar set, the control operator manually rephases the intruding radar set's output to prevent interference between the two sets.

Automatic phasing provisions are currently being incorporated in most FPQ-6, FPS-16, and Sperry (ARIS) radar sets. A radar set operating in the automatic phasing mode senses for occurrence of pulses in two time regions; one prior to arrival of the beacon reply pulse sent in response to that radar set's interrogation pulse, the other following receipt of the beacon reply pulse. If occurrence of a pulse within either of these regions is detected during a specific number of consecutive interrogation-return pulse cycles, the radar set first seeks out a region within the range interval such that no pulses would be detected prior to or following a beacon reply pulse. The set then automatically phase shifts the transmission so that the return will occur in the desired region.

Speech pulses could occur within these regions in a random fashion. If a significant number occurred within consecutive regions the radar would be forced to rephase. The possible presence of speech pulses in the regions between beacon reply pulses may result in the radar equipment being unable to rephase and it may have to shut down.

Furthermore, the design of the Astrovoice encoder is such that it may transmit a tag, or delayed pulse at a fixed time following beacon transmission of a reply pulse. The tag pulse is used to enable the decoder to identify the reply pulse and prevent its being decoded as a speech pulse. The tag pulse, if transmitted, will always occur within the period during which the radar set operating in the automatic phasing mode is sensing for occurrence of pulses prior to and following the beacon reply pulse. As a result, if a large number of tag pulses were generated the radar set would be forced to change its phase and the presence of speech pulses may cause radar shutdown, as noted previously. If the encoder were modified to inhibit speech pulse transmission during the period in which the radar equipment is sensing

for pulses in the pre- and post-beacon pulse intervals, speech pulses could not be transmitted when more than one tracking radar set is interrogating the beacon.

On the basis of this investigation and discussions with Atlantic Missile Range personnel, it was concluded that while the automatic phasing capability, as well as the automatic acquisition capability, is desirable, it is a necessity only in an emergency.

The modification proposed here to allow speech pulses to be inhibited when the radar equipment is operated in the automatic acquisition mode can also be used to prevent continual phase shifting when the radar set is operating in the automatic phasing mode. Essentially, manual phasing would always be used except when emergency conditions indicate that the equipment must be operated in the automatic phasing mode. At that time any radar set capable of transmitting pulse code groups could be used to inhibit speech pulses by transmitting a suitable code group to the beacon.

5.5.1.5 Interference Zone Tracking

When the target passes through a region of space such that the sum of:

1. The travel time of the ground pulse from the radar set to the target

plus

2. The travel time of the beacon reply pulse transmitted in response to the ground pulse

equals an integral multiple of the given pulse period, the beacon reply pulse will be prevented from entering the radar set receiver. It will be blocked by a ground pulse which is being transmitted coincident with the time of arrival of the reply pulse. The regions of space where this condition occurs are known as interference zones.

An appropriate technique has been developed, however, to allow tracking even through the various interference zones. In this technique the ground pulse transmission time is either advanced or delayed for a time sufficient to allow the beacon reply pulse to be received. The technique is usually described as the phase-jumping technique in that some ground pulses are transmitted in phase with a basic clock pulse train while other ground pulses are transmitted in a fixed phase position (leading or lagging) relative to the basic clock pulse train. Whether the ground pulses lead or lag depends upon the manufacturer's approach to design of the particular type of radar equipment.

Figure 5-76 demonstrates the timing involved in using the phase jumping technique when the sum of the travel times is equal to twice the basic pulse period, as shown at A, or is exactly equal to the basic pulse period, as shown at B. The same technique can be extended to cover other situations where the travel time is N times the basic pulse period.

Figure 5-76 also indicates the inhibit intervals used to prevent speech or sync pulses from interfering with reception of ground pulses at the beacon. The inhibit intervals are produced by the encoder as described in paragraph 5.3. As Figure 5-76 indicates, however, such inhibit intervals would be ineffective in protecting the ground pulses from interference when the radar set is tracking a target located in the first interference zone (located at a range of approximately 500 nm when a pulse rate of 160 pps is used). As a result, lockout of up to 20% of the ground pulses could occur. If such a lock-out percentage is too high, the encoder can be modified to provide the inhibit interval at a time twice the basic ground pulse period (2T) away from the time at which the ground pulse is received at the beacon. This modification will prevent lock-out of ground pulses by providing appropriately-timed inhibit intervals for all pulses received at the beacon.

Difficulties in regard to timing of the inhibit intervals in the second interference zone (located at a range of approximately 1,000 nm for a 160 pps pulse rate) can be overcome in a similar manner by providing the inhibit intervals at a time four times the basic ground pulse period (4T) away from the time at which the ground pulse is received at the beacon.

If lock-out of 20% of the ground pulses is considered to be unacceptably high, and tracking and communication is to be accomplished through more distant interference zones, the basic approach described above could be extended. However, the modifications necessary to change the time of the inhibit intervals would be cumbersome. Instead, a special sampling-type logic can be provided to generate inhibit intervals suitably timed for various interference zones. One difficulty complicating design of such a logic system is lack of standardization in the design of radar equipment, particularly in regard to application of the phase-jumping technique. In some sets a phase jump lead is used while in others a phase jump lag is used.

5.5.2 Astrovoice/Beacon Interface

5.5.2.1 Probable Beacon Types

Basic criteria for selecting a radar beacon, or transponder, for operation with the Astrovoice II system include:

1. Short recovery time
2. Maximum allowable continuous pulse repetition rate.

The type AN/DPN-66 beacon appears best able to satisfy these criteria. Its recovery time is 50 μsec, maximum. Its maximum allowable pulse repetition frequency (prf), for a 0.75 μsec wide pulse, is 2,670 pps.

A duty cycle limit of 0.002 is specified for the magnetron in the beacon by the magnetron manufacturers. Although it is known that this limit can be extended for short periods, manufacturers are reluctant to publish any figures

indicating short-time duty cycle limits. The AN/DPN-66's prf can be safely increased to 4000 pps by reducing the pulse width to 0.25 μsec. This rate is well within the duty cycle limit of the magnetron.

Manufacturers of radar beacons have generally included over-interrogation protection circuits in the beacons to limit transmissions from the beacon as a means of preventing the magnetron duty cycle limit from being exceeded. These circuits are generally of the time constant type. They control the long-term duty ratio of the magnetron by integrating over several incoming pulses and feeding back a signal used to inhibit pulses during a fall-time interval.

It is recommended that any beacon to be used in conjunction with the Astrovoice II system be provided with over-interrogation circuits to protect the magnetron.

5.5.2.2 External Connections--Astrovoice to Beacon

The Astrovoice II system requires connection between the beacon and the encoder system to:

1. Detect receipt of ground pulses.

2. Enable speech and sync pulses to be transmitted by the beacon.

Both of these connections may be made to a common point.

Beacons other than the AN/DPN-66 require slight modification to provide the necessary connections.

The AN/DPN-66 beacon is equipped with two external contacts (identified as "test trigger input" and "test trigger output" contacts). Both contacts are accessible in a single power plug through which the necessary connections between the beacon and the Astrovoice encoder system can be established. The trigger input and output contacts are provided to facilitate checking operation of the beacon. The test trigger input signal is used to trigger the beacon transmitter which responds by transmitting a beacon reply pulse. The test trigger output signal is produced by the beacon receiver in response to detection of a ground pulse. In order to trigger the beacon properly, the test trigger input signal must be a 4-volt, 1.5 μsec pulse driven from a 50 ohm impedance. The test trigger output signal provided by the beacon receiver is a standard-type, 2-volt (minimum) pulse driven out of a 100 ohm impedance. The test trigger output signal occurs prior to the beacon's ground pulse decoder insofar as the beacon's internal circuit arrangement is concerned. Any detected ground pulse produces a video output signal which appears at this point (as a test trigger output signal) prior to its application to the input terminal of the beacon's decoder. The trigger output signal is of particular value if commands in the form of radar pulse code groups are to be transmitted from the radar tracking equipment to the spacecraft to inhibit transmission of speech and sync pulses, as noted in paragraph 5.5.1.5.

Manufacturers of other beacons give assurance that only a simple modification is required to enable addition of the required connectors to their beacons.

5.5.2.3 Operational Considerations

Laboratory experiments were performed in which speech pulses were transmitted via an ACF type 149C-5 beacon at an average pulse repetition frequency (prf) of 3700 pps. The beacon was operated at this rate for several days without significant degradation in its performance even though it did not have a protective circuit to prevent the magnetron duty cycle from being exceeded.

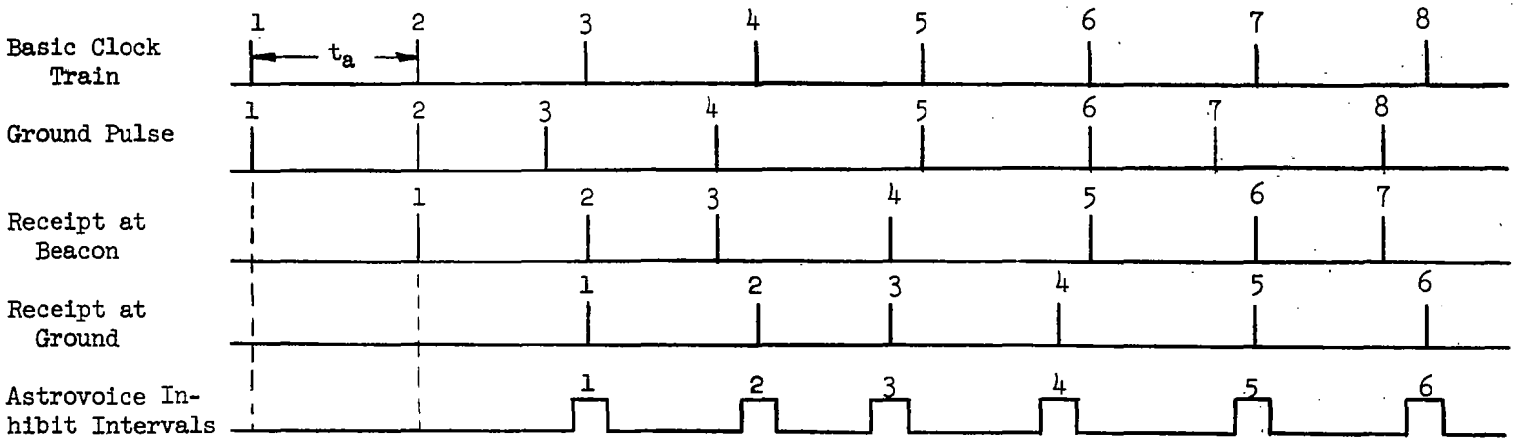
During subsequent experiments in which a VOX (voice operated transmission) circuit was simulated, the average prf was reduced to 2800 without significant degradation of the audio signal quality. Incorporation of a VOX circuit in the encoder of operational Astrovoice systems is recommended.

Results of intelligibility tests indicate that inhibiting of speech pulses by tracking radar equipment transmissions does not significantly degrade the intelligibility of the speech. These results were noted during and after tests in which the effects of simultaneously interrogating the beacon by three different simulated tracking radar sets were evaluated. The equivalent pulse rate was 426 ground pulses per second.

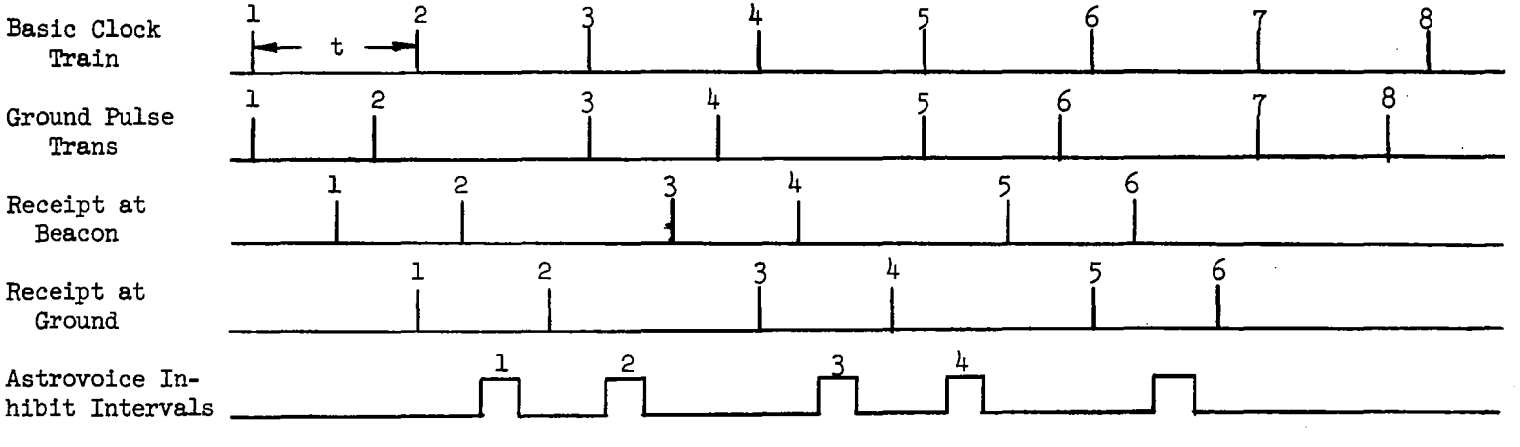
The intelligibility tests conducted on the Astrovoice system were made on the basis of simultaneous interrogation of the beacon by three different radar sets. It was considered that this represented a more realistic situation than one based on simultaneous interrogation of the beacon by a greater number of radar sets.

While it might be supposed that the presence of simultaneous interrogation pulses from several radar sets would greatly increase the average pulse repetition frequency of the pulses entering the beacon in comparison with the average prf of speech pulses entering the beacon and, as a result, cause the over-interrogation circuit to operate to reduce the average prf, such was not quite the case. The inhibit intervals provided before and after each ground pulse can inhibit more than one speech pulse. The increase in the average prf is, therefore, not a linear addition. Actually, by appropriately optimizing the design, a slight reduction of the average prf could be achieved even though the beacon were being interrogated simultaneously by three tracking radar sets.

It should be noted that a VOX circuit need not be employed if the pulse widths can be reduced, for example, to 0.25 microseconds. Such a reduction in pulse width allows use of a correspondingly higher prf for the same magnetron duty ratio.



(A)



(B)

Figure 5-76. Timing Diagram, Two-Way Travel Time: A, Twice Basic Pulse Period; B, Equal To Basic Pulse Period

5.6 SPEECH INTELLIGIBILITY

5.6.1 Introduction

The Human Factors Department of Avco/RAD conducted a study of the Astrovoice Communication System to determine the intelligibility index. This study was conducted in accordance with the direction provided by Contract NASW 586. Since the contract referred to above is only for a feasibility study, the scope of the investigation was necessarily limited. No attempts were made to determine if there were syllabic distortions, omissions, or additions, nor were extensive attempts made to relate the findings to the literature on communication theory. Additionally, it was not possible to undertake a subject training program involving a great number of trials. However, comparisons of the Avco Astrovoice system intelligibility index with three other communication systems was accomplished[1]. These comparisons were with the analog, constant frequency sampling, and clipper audio communications systems.

5.6.2 Procedure

The Harvard phonetically balanced (PB) word lists were recorded on magnetic tape by two untrained male speakers employing a volume unit (VU) meter for monitoring. The interval between each stimulus word and the beginning of the next carrier phrase was five seconds. Each speaker recorded each list a total of ten times. The words were randomized within the list and the lists were recorded in random order*. The recordings were made after the output was passed through a filter which removed sound below 260 cycles per second (cps) and above 4 kilocycles per second (kc/s) to insure all output was within the undistorted frequency spectrum of the recorder.

The test items were played back over earphones** to untrained male subjects isolated in a quiet room. The sound pressure levels*** were equaled during playback. The average background noise and peak speaker volume are presented in Table 5-3. The volume was judged by the listeners to be both comfortable and adequate. Testing sessions were limited to one hour, including a five-minute rest period between the presentation of each word list.

5.6.3 Results

The data collected in this study was first analyzed to determine the effect of word list learning and increased subject sophistication in intelligibility test taking. Of the five communication systems tested, the analog system exhibited the highest signal-to-noise ratio (SNR); therefore, learning and sophistication would be most clearly exhibited in the by-trial results of this system. The by-trial scores in Figure 5- 77 , System 2, show that the effect of word list and subject sophistication is negligible. However, a subject's ability to discriminate between signal and noise within a system does improve (Figure 5- 77 , Systems 1, 3, 4, 5).

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[1] Reference 1, Bibliography (See Appendix A).

* A Wollensack T1515-4 tape recorder and microphone was used for all recording and playback.

** Koss Earphones Model SP3X

*** Sound pressure levels were taken by placing an Altec Microphone 633A amplified by a General Radio Microphone Transformer 759-26 directly against the earphone. Sound pressure levels are those indicated on General Radio Sound Level Meter Type 1551-A.

Table 5-3

Sound Pressure Measurements of Stimulus Tapes

Taken at Each Earphone

Communication System	Background Noise	Peak Speaker Volume (in db)
1. Astrovoice w/o inhibits	74	88
2. Analog	61	88
3. Astrovoice w/inhibits*	73	88
4. Frequency sampling	67	88
5. Clipper Audio	84	88

* The inhibits represent 3 radar sets with pulse rates of 142 pulses per/sec each.

The differences between the five systems were analyzed through a factorial analysis of variance. The summary table of this analysis is presented in Table 5-4, which shows significant difference among systems, subjects, and speakers.

The performance variations among subjects on the five systems is shown in Figures 5-78, 5-79, 5-80, 5-81, and 5-82. A Duncan multirange test was run to isolate the significant subject differences (Table 5-5). The results shown on Table 5-5 point out one subject (C) as being the primary contributing cause of the significant subject variations.

The differences between the two speakers across all five systems is presented graphically in Figure 5- 83 . The overall stimulus-to-error ratio (SER) was significantly higher for speaker 1 but it varied across systems. The comparison of the five systems according to mean number of errors per system per trial and the mean intelligibility index per system are given in Table 5-6.

As expected, analog and frequency sampling displayed significantly higher intelligibility indices. However, the intelligibility index of the Avco Astrovoice communication system is such that we could expect a great deal of information to be transmitted.

5.6.4 Discussion

The foregoing analysis pointed out the following significant differences: 1) between speakers, 2) between subjects, and 3) between systems.

The significant difference between the two speakers was assumed to be caused by one or more of the following factors: 1) differences in timber of voices; 2) accent; or 3) training in speaking. However, both speakers were judged to have similar if not neutral accents, and both had comparably deep speaking voices. It must be concluded then, that the interspeaker differences were due to differences in the levels of training and experience in speaking. Some additional observations, while not experimentally verified, have caused conjecture that differences of voice timber would result in different intelligibility scores, and further, that higher pitched voices (e.g., female) would lead to much greater intelligibility.

As pointed out in the results, one subject caused the significant variation among subjects. It was discovered after the test that this subject had previously participated in intelligibility testing.

An examination of the intelligibility curve for the analog system (see Figure 5- 77) would seem to indicate that there is little learning of word lists or testing procedure sophistication. Therefore, it can be assumed that word list learning and testing sophistication are not present in the intelligibility indices or the intelligibility curves of any of the systems.

From an examination of the curves presented by Pollack[3] the second derivative of the learning curves, for intelligibility of words in a noisy field, occurs

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[3]Reference 3, Bibliography (See Appendix A.)

Table 5-4

Summary Table of Main Effects*

Source	d.f.	Sums of Squares	Mean Squares	F
Systems	4	1285.72	321.43	25.35**
Subjects	3	177.48	59.16	4.66**
Speakers	1	144.5	144.5	11.39**
Systems by Subjects	12	95.28	7.94	-
Subjects by Speakers	3	6.66	2.22	-
Systems by Speakers	4	121.86	30.46	2.40
Systems by Subjects by Speakers	12	22.27	1.86	-
Within	160	2030.31	12.68	-
Total	199	3884.08	-	-

* An analysis of word lists by systems, subjects, and speakers showed that performance between word lists was not significantly different; therefore, word lists were dropped as a main source of error.

** Significant at the 0.01 Level.

Table 5-5

Duncan Multi-Range Test Between Subjects

	Subject			
	C	D	A	B
Mean No. of Errors	3.92	4.22	4.94	6.36

The means not underscored by the same line are significantly different.

Table 5-6

Duncan Multi-Range Test Between Systems

System	Mean No. Error	Intelligibility (Percent Articulation)
Analog	0.90	99%
Constant Frequency Sampling	2.87	95%
Astrovoice with Radar	6.3	90%
Astrovoice Without Radar	6.72	89%
Clipper Audio	7.5	88%

The means not connected by the same line are significantly different.

at approximately the 10th repetition (irrespective of feedback information). If this is true, the Astrovoice communication system is just approaching its first learning plateau and the intelligibility index is probably higher than the indicated 90%. A mean intelligibility index was computed for the last three trials of each communication system. These means are presented in Table 5-7.

From Table 5-7 and the above discussion, it can be seen that the increase in intelligibility can be attributed to subject familiarity with the system.

A matter of concern was the contractual request to use the Harvard PB word list. Frequency of word usage has been demonstrated to be a most important variable in the computation of intelligibility indices [4,5]. Rosenzweig and Postman[6] found that frequency of usage of words accounts for about one half the variance of the intelligibility threshold of words in a noise field. Howes[2] states that "observer's experience with a word as a distinctive unit appears to be the primary determinant of its intelligibility". Howes[2] further points out that only 14% of the words in the Harvard PB word list have a Lorge magazine frequency count of 1000 or more.

A test procedure utilizing more familiar words or conducted over a longer period of time would probably disclose an intelligibility index significantly higher than the obtained 90%. In view of the above factors and because Astrovoice-type communication systems have potential theoretical implications, it is felt that additional research in this area would be very fruitful.

[4,5] References 4 and 5, Bibliography (See Appendix A.)
[6] Reference 6, Bibliography (See Appendix A.)
[2] Reference 2, Bibliography (See Appendix A.)

Table 5-7

Mean Intelligibility Index for Trials 8, 9, and 10

System	Mean Intell. Index
Astrovoice without inhibits	91%
Analog	97%
Astrovoice with inhibits	96%
Frequency Sampling	97%
Clipper Audio*	87%

* The figures from clipper audio are probably not representative since all of the subjects complained quite a bit about the distressing noise between stimuli.

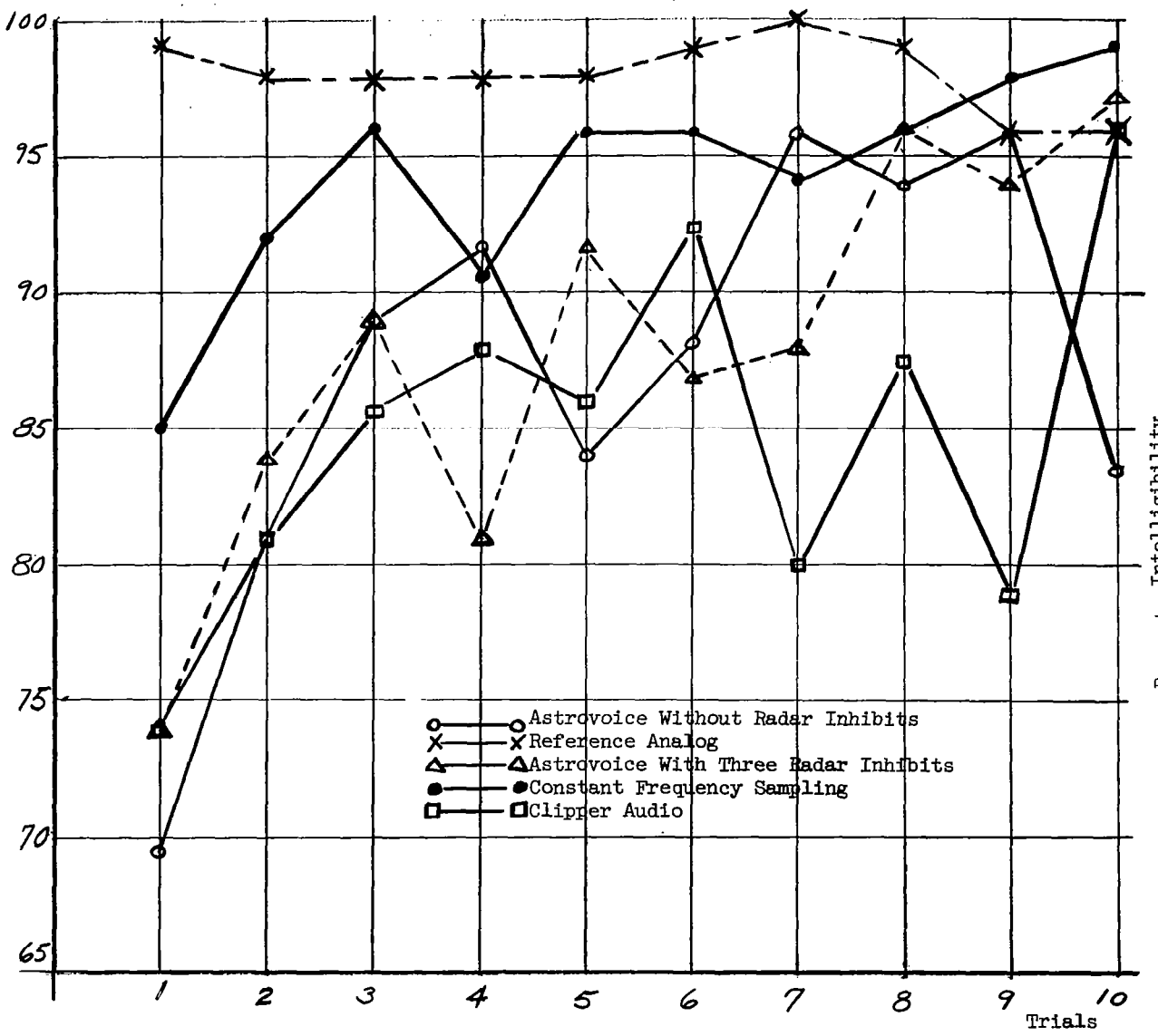


Figure 5-77. Intelligibility Indices (Systems X Trials)

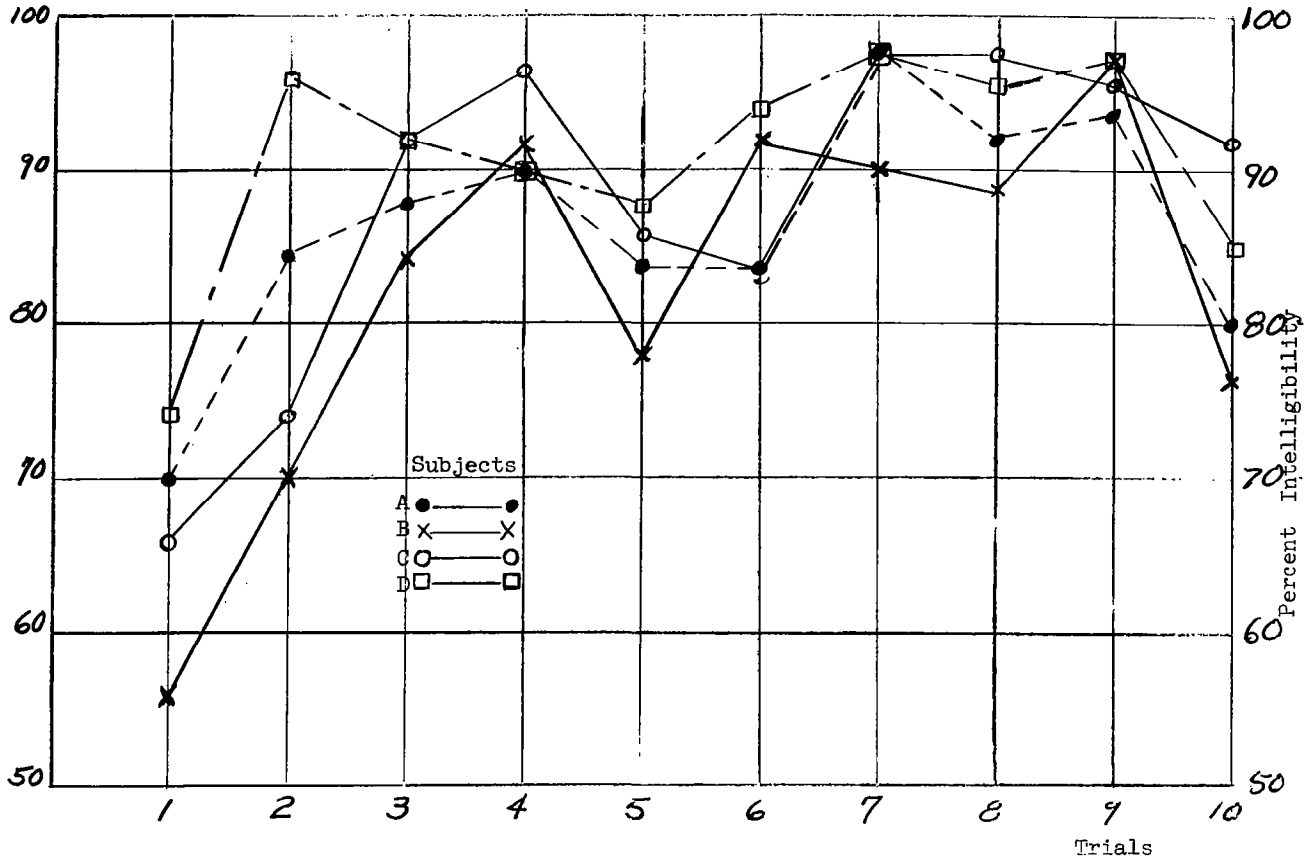
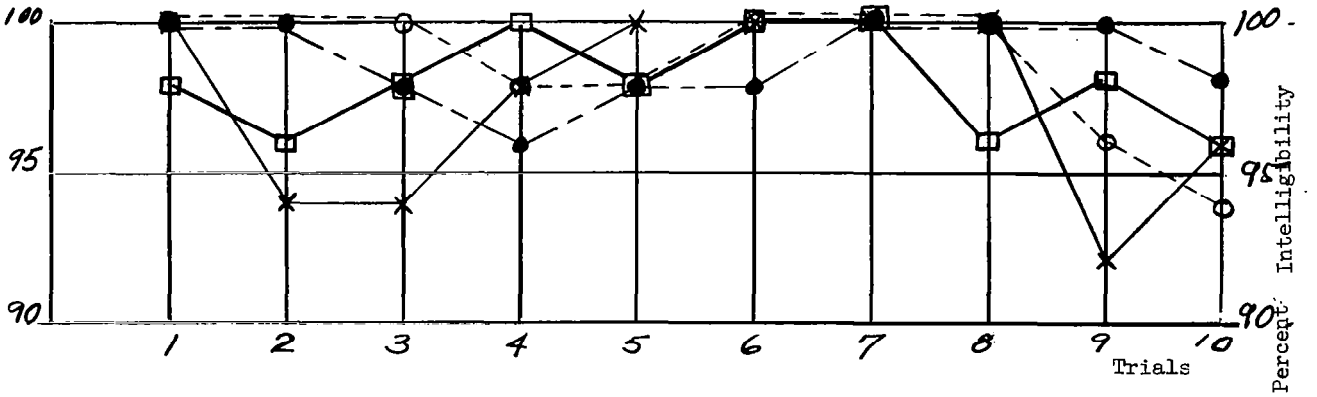


Figure 5-78 . Intelligibility Indices (Systems X Subject X Trials)
Avco Astrovoice Without Radar Inhibits



Subjects

A
B
C
D

NOTE: To simplify interpretation of data, the intelligibility scales used on Figures 5-79 and 5-81 represent an expansion of the upper portion of the intelligibility scales used on Figures 5-78, 5-80, and 5-82.

Figure 5-79 . Intelligibility Indices (Systems X Subject X Trials) Reference Analog

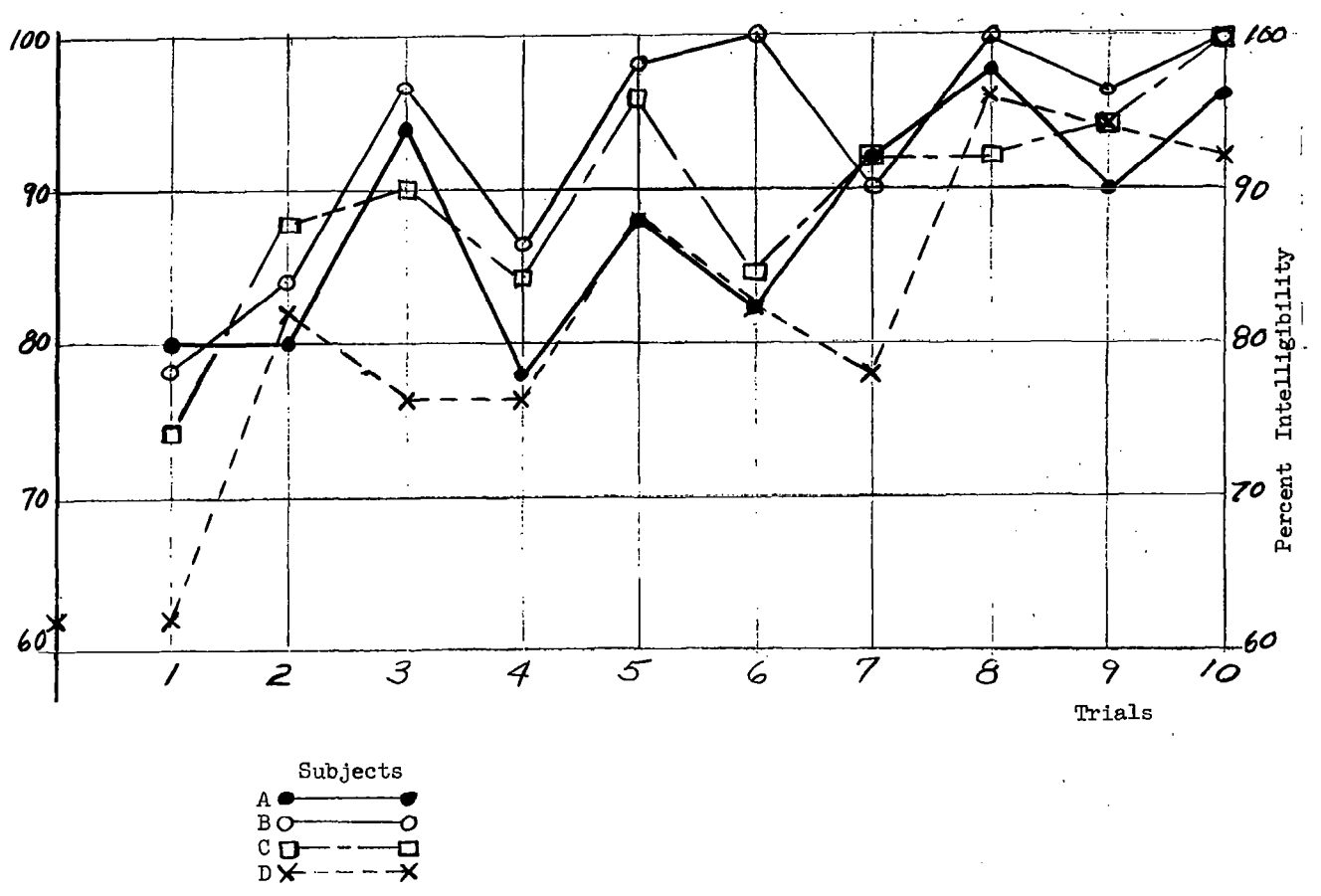
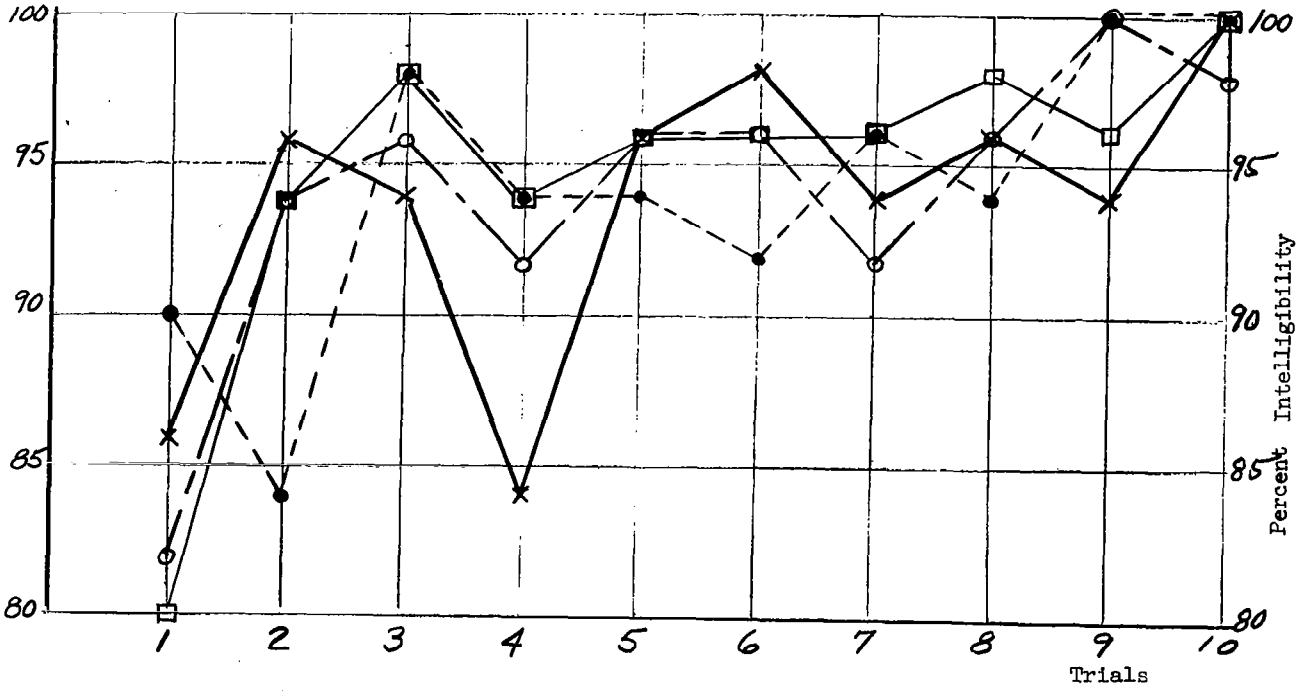


Figure 5-80 . Intelligibility Indices (Systems X Subject X Trials)
Avco Astrovoice With 3 Radar Inhibits



NOTE: To simplify interpretation of data, the intelligibility scales used on Figures 5-79 and 5-81 represent an expansion of the upper portion of the intelligibility scales used on Figures 5-78, 5-80, and 5-82.

Subjects
A
B
C
D

Figure 5-81 . Intelligibility Indices (Systems X Subject X Trials)
Constant Frequency Sampling

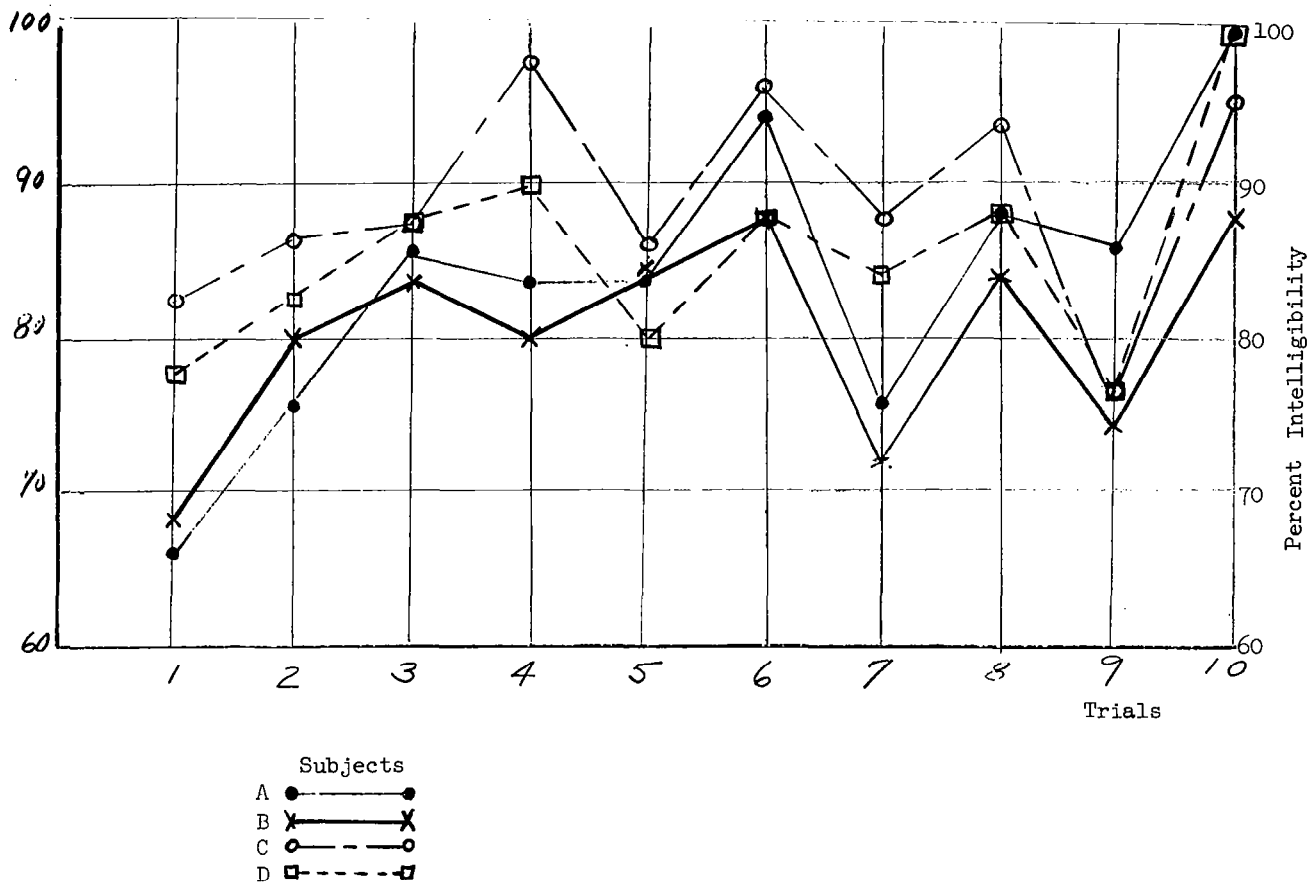


Figure 5-82 . Intelligibility Indices (Systems X Subjects X Trials)
Clipper Audio

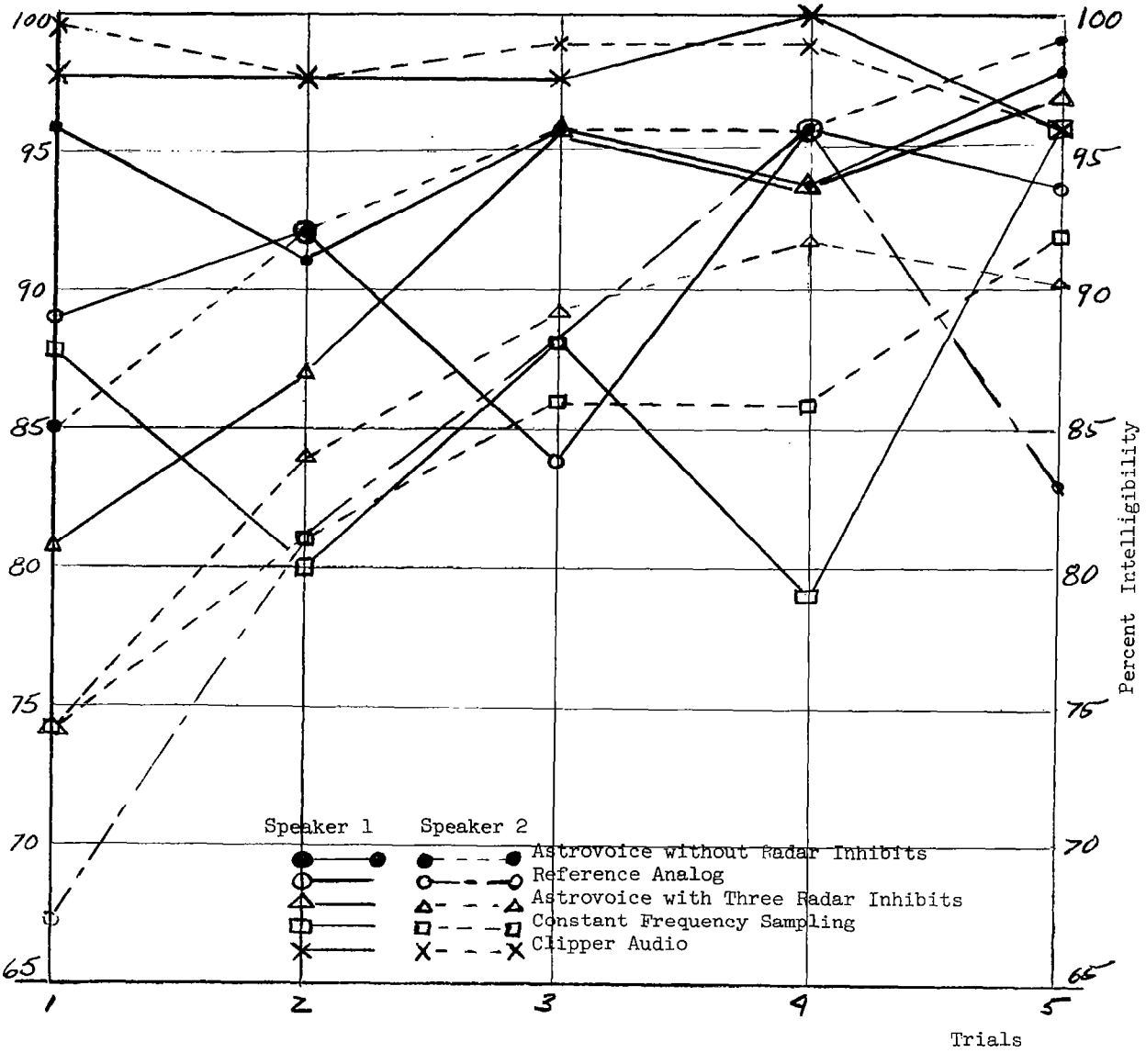


Figure 5-83 . Intelligibility Index Scores (System X Speaker X Trials)

APPENDIX A

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5.7 SYSTEM PERFORMANCE

5.7.1. Experiments and Results

5.71.1. Pulse Rates

Magnetic tape recordings of the voices of various Astronauts were made available to Avco-RAD by the National Aeronautics and Space Administration (NASA) and were played through the Astrovoice II system. Analysis of the encoder transmission rate indicated that the average pulse repetition frequency (prf) was approximately 3700 pps. A significant portion of this pulse rate was found to be due to ambient noise present during inter-word and inter-sentence spaces.

Although the pulse repetition frequency can be reduced by using less gain in the system, thereby decreasing system sensitivity to ambient noise, such an approach tends to degrade speech intelligibility. Peak-to-peak (p-t-p) consonant voltages are relatively low in comparison to p-t-p vowel voltages. Consequently, a reduction in system sensitivity would cause some consonant voltages to be below the system's input threshold level. As a result, adjustment of system sensitivity to eliminate ambient inter-word and inter-sentence noise when the level of such noise is high would compromise speech intelligibility, particularly in the case of consonants at the beginning of words or sentences. As high a gain as is practical, therefore, is desirable from the standpoint of speech intelligibility enhancement.

It is recommended, therefore, that use of a fast-acting, voice-operated transmission (VOX) circuit in combination with a suitable squelch circuit be investigated. Incorporation of such a system would reduce the pulse repetition frequency due to inter-word and inter-sentence ambient noise while at the same time it would allow use of a high gain level to enhance intelligibility. A simulated VOX/squelch circuit was constructed in breadboard model form and tested. Test results indicate that the average prf could be reduced to approximately 2800 pps without, in Avco-RAD's opinion, seriously degrading speech intelligibility. Further investigation in this area is recommended.

Obviously, the degree of improvement in intelligibility using a VOX/squelch circuit is determined, to a great extent, by the level of the ambient inter-word and inter-sentence noise.

5.7.1.2 Intelligibility Tests

Detailed intelligibility tests were performed by the Avco-RAD Human Factors Department. These tests were made relatively late in the program. Although actual magnetic tape recording of data required for the intelligibility tests took little time, the recordings had to be made well in advance of the completion date of the Astrovoice program to allow time for the tests themselves, which were known to be time consuming.

Subsequent to recording data for the intelligibility tests, various system modifications (principally in the area of limiting or removing noise in certain noise-producing circuits) were incorporated. Because the recordings made for

the intelligibility tests had to be made before the system was modified and improved, test results are not indicative of performance of the system as finally developed. In addition, the recordings of system performance on these tapes do not correspond in quality to recordings sent to NASA to demonstrate system performance since the latter recordings were made subsequent to system modification.

While it is difficult to predict the results if intelligibility tests were to be conducted on the improved, less noisy, system, Avco-RAD feels that the intelligibility index would be found to have been increased as a result of incorporating the various modifications. Unfortunately, time did not allow conduct of intelligibility tests on the improved system.

During the intelligibility tests, described in paragraph 5.6 of this report, a comparison was made between the intelligibility of unprocessed speech and that of speech processed by four alternative systems. The systems were:

1. Synchronous rectangular audio
2. Synchronous rectangular audio with some pulse position modulation pulses deleted by simulating simultaneous interrogation of the beacon by three tracking sets.
3. Constant frequency sampling at a sampling frequency of 6 kc/s.
4. Clipper audio.

Detailed test results are presented in paragraph 5.6.

5.7.1.3 Circuit Performance

Over-all circuit performance was found to be excellent. Some circuit sources of noise were discovered, however, as follows.

1. Timing errors resulting from incomplete recovery of the pulse modulation monostable multivibrator used in the encoder speech processing subsystem were found to cause distortion of the decoder output when the audio input signal level was low. The level is low, for example, during inter-word and inter-sentence spaces. This phenomenon, often referred to as timing-to-amplitude cross-talk, results from a residual effect in the multivibrator capacitor. The effect is related to the time of previous firing of the multivibrator (and capacitor discharge which occurs at that time). As a result of this phenomenon, low level ambient inter-word and inter-sentence noise tended to appear amplified at the output of the decoder. In addition, it was found that the timing-to-amplitude cross-talk caused some distortion of low level peak-to-peak consonant voltages.

2. The same type of timing-to-amplitude crosstalk also introduced some noise when pulses from the encoder system were passed through an ACF 149C radar beacon, or transponder, to the decoder system. As a result of the crosstalk, ambient noise at the decoder output was increased. The noise was in the nature of a hissing sound. The type of lock-out circuit used in the beacon was found to be the source of the cross-talk. The problem appears to lie in the exponential recovery characteristics of the bias circuit associated with a silicon-controlled rectifier used for triggering purposes in the beacon and can easily be overcome by incorporation of a different beacon driving circuit in the encoder.

5.7.1.4 System Modifications

Although many modifications were made in the system in the course of the program, two are particularly noteworthy because of the significant effect they had on system performance. Descriptions of these modifications follow.

1. Adjacent Sampling Pulse Separation. The system was modified to facilitate sampling and, in effect, allow sampling adjacent peaks and troughs at a rate equivalent to a 9 kc/s rate without significant increase in the actual pulse repetition frequency. The modification included reduction of the encoder system post-inhibit period to a point at which only one clock pulse was inhibited instead of the two pulses which had been inhibited previously. The decrease made it possible for adjacent samples to be taken when necessary and resultant speech pulses to be transmitted with a separation of as little as 110 μsecs between samplings. This is effectively equivalent to a 9 kc/s sampling rate. This modification produced a significant increase in the quality of the processed speech without a significant increase in the average frequency of the transmitted speech pulses.

2. Non-Signal-Correlated Sampling. The encoder speech processing subsystem was modified to incorporate a technique for providing non-signal-correlated samples of the audio input waveform. This technique and the reason for its use are described in paragraph 5.3.2.1.4.2.2. Analysis of experimental data regarding system performance indicated that adoption of this technique effects a substantial increase in both the quality and intelligibility of the processed speech without an increase in the average frequency of the transmitted speech pulses.

5.7.2 Comparison of Various Speech Processing Systems

Three different types of speech processing systems were each compared with the synchronous rectangular audio (SRA) type of speech processing system. Results of the comparisons are described in paragraph 5.7.2.1 through 5.7.2.3.

Development of the synchronous rectangular audio speech processing system represents development of a speech processing approach which is based upon direct retention of amplitude and frequency information contained in the speech waveform. The major advantage of the SRA speech processing system lies in the fact that the sampling frequency is derived from the signal itself.

5.7.2.1 Synchronous Rectangular Audio Versus Clipper Audio

Speech processing systems of the clipper audio type process speech by greatly amplifying the audio input to the system and then forming a constant amplitude square wave model of the input waveform. A regenerative clipper circuit is used to form the square wave model.

It is generally believed that the frequency (zero crossing) information contained in the input waveform is preserved while amplitude information is lost when a clipper audio type speech processing system is used. However, investigations made prior to and during the course of the Astrovoice II program indicate that although much of the amplitude information is lost in the clipping process, a significant portion of it is, in fact, preserved in the form of duty ratio modulation.

It can be demonstrated that when high and low frequency waveforms are superimposed and applied to a clipper, the low frequency waveform will pass through the clipper circuit and can be detected at the output of the clipper in the form of a duty ratio modulation of the high frequency rectangular output waveform. It is felt that this effect contributes significantly to the intelligibility of speech processed through a clipper audio type system.

Relatively high frequency, low volume inter-word and inter-sentence ambient noise, when processed through the clipper circuit, produces loud and annoying noise at the output of a clipper audio system. Although the input sensitivity of the system can be reduced to reject such noise, speech quality and intelligibility is concurrently compromised through loss of the relatively low peak-to-peak voltage levels of consonants at the beginning of words and sentences. Experiments have shown that the intelligibility of speech processed in a clipper audio system is seriously degraded when this approach to noise reduction is adopted.

The deletion of pulses from transmission when a clipper audio system is used causes phase reversals in the audio signal in the decoder. Such reversals seriously degrade both quality and intelligibility of the processed speech.

In comparison to clipper audio, synchronous rectangular audio is not subject to phase reversals and the ratio between the speech signal level and the inter-word and inter-sentence noise signal level at the output of the decoder is essentially the same as the corresponding ratio at the input of the encoder. A VOX/squelch circuit is used to reduce the average pulse rate in the SRA system.

5.7.2.2 Synchronous Rectangular Audio Versus Constant Frequency Sampling

In the constant frequency samplying (CFS) type of speech processing system the amplitude of a speech waveform is sampled at times determined by a clock pulse train. Information regarding the amplitude at the time of sampling can then be encoded according to a suitable pulse position modulation scheme and the resultant pulses transmitted to a decoder. In the modulation scheme the transmitted pulses are time modulated with respect to pulses in the clock pulse train. At the decoder a second clock pulse train operating synchronously with the encoder clock pulse train is used to extract the amplitude information and an approximation of the encoder input waveform is constructed. The degree to which the decoder output waveform approximates the encoder input waveform is a function of the sampling pulse rate. As the rate is increased the approximation approaches the input waveform.

Experiments were made on constant frequency sampling speech processing systems during the course of the Astrovoice II program and the following points were noted:

1. At sampling pulse rates of 20 kc/s, the difference between CFS-processed speech and unprocessed speech is almost imperceptible.

2. As the clock pulse rate is decreased, CFS-processed speech acquires a scratchy quality, as if the high frequency response were being greatly emphasized.

3. At clock pulse rates below 4 kc/s, CFS-processed speech acquires an "inverted speech" effect similar in sound to that produced by an improperly tuned sideband signal. Such a sound can be observed from communications receivers. The impression is given that the speaker is attempting to talk "with a mouth full of marbles".

4. At a clock pulse rate of 6 kc/s CFS-processed speech is superior in quality to SRA processed speech. It should be noted that this is the rate used for CFS-processed speech during the intelligibility tests.

5. At a clock pulse rate of 5 kc/s, CFS-processed speech is approximately equivalent in quality to SRA-processed speech.

6. At a clock pulse rate of 3 kc/s, CFS-processed speech is completely degraded and, in effect, unintelligible.

Comparison between SRA and CFS processed speech of equivalent quality indicated that if an optimized SRA processing system is used (that is, one incorporating a VOX/squelch circuit thereby permitting a reduction in the average pulse repetition frequency to approximately 2800 pps) there is a 2 to 1 pulse rate advantage in favor of SRA. If, however, background noise processed along with the speech reaches a significant level with respect to speech levels, the VOX/squelch circuit cannot then be used in the SRA system and the advantage in pulse rate in favor of SRA processed speech becomes 4 to 3.

5.7.2.3 Synchronous Rectangular Audio Versus Triangular Audio

The difference in the amount of distortion of the audio input waveform introduced by the SRA and by a conceptual triangular audio (TA) speech processing system may be described as follows. The latter system is still in the conceptual stage, however, and would require development and test.

If the facsimile waveform produced by a synchronous rectangular audio processing system is subtracted from the audio input waveform from which the facsimile was constructed, the resultant waveform would indicate the amount of distortion introduced by the SRA processing system.

If, however, a triangular-type facsimile of the audio input waveform were constructed in such a fashion that it retained as peaks and troughs the original amplitude and frequency of the audio input waveform, and the audio input waveform were then subtracted from the facsimile waveform, the resultant waveform would represent distortion introduced by the triangular audio processing system.

Comparison of the resultant waveforms (those indicating the distortion produced in each system) would indicate that significantly less distortion is introduced by the triangular audio processing system and it can, therefore, be concluded that the latter system is superior in performance.

Development of a triangular audio speech processing system requires that:

1. The voltage difference between two successive samples be determined accurately.

2. The voltage difference be divided by the time interval between these same samples.

From this information the slope to be applied in producing various portions of the facsimile waveform would then be derived.

If the time intervals between successive samples are equal, as in the case in constant frequency sampling, nothing more is required for performing these functions than a time delay between the input and output. If the time intervals between samples are not equal, as is the case in the signal-correlated sampling method, a complicated information storage technique would be required.

A modified version of a triangular audio speech processing system (N + 1 triangular audio) can be developed in which the voltage difference between the amplitude of the waveform at either end of a time interval, divided by the magnitude of the time interval, will define a slope to be applied during the next succeeding interval. This technique was investigated and studied during the Astrovoice II program. It was not, however, implemented. Avco-RAD considers that further investigations in this area are warranted.

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